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Design of flash memory arrays with SOI cells utilizing the back-channel based erase method

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This paper demonstrates one way of designing a flash memory array which incorporates cells produced in Silicon-On-Insulator (SOI) technology. General principles of SOI flash memory cell operation are presented. SOI memory cells used in the design utilize a standard way to write information and a novel method to erase it. Performance analysis of the suggested design is carried out for a simple memory array. 16x16 memory chip layout is presented as an example.

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1. Introduction

Nonvolatility, fast updateability, and high density of flash memories rank them among the most used solid-state memories of today. Flash memory chips are available in densities much higher than any EPROM or EEPROM. Another big advantage of flash memory is that it can be erased a block at a time and programmed a bit at a time [1,2,3]. In electronic devices which incorporate SOI based memories ultra-fast HFET transistors can be used [4,5].

2. General principles of SOI memory cell operation

Flash memory cell is usually programmed by charging the floating gate via hot carrier injection and erased through Fowler-Nordhaim (FN) tunneling of charge from the floating gate. An important thing to consider in the design of a memory cell which makes use of hot carrier injection is the voltage applied between its terminals (source, control gate and drain), since the injection of hot carriers to the floating gate depends on the lateral electric field in the channel and pinch-off region. The electric field must be high enough to provide carriers with sufficient energy. Electron energy distribution needs to be shifted to much higher values compared to the case when they are in equilibrium with the lattice.

If a memory cell is not properly erased it may give rise to errors during subsequent use. Erasing based on FN tunneling does not enable proper control of floating gate charge and gives rise to a high dispersion of threshold voltage distribution after erasure. If a cell is over-erased, programming may produce a negative threshold voltage, leading to an error at readout. There are several different approaches for solving this problem: 1) high voltage source with grounded gate erase, 2) negative gate with positive source erase, 3) negative gate with grounded channel erase [6,7,8]. These methods are compared in [9] and they all include iterative erase and verify sequences with pre-programming of all bites to obtain a tight distribution of threshold voltage. Some improvements can be achieved with the self convergence erasing method [10].

Fig. 1 illustrates the principle of writing information into a SOI memory cell. The cell is programmed by keeping the control gate at a large enough voltage and simultaneously applying a voltage pulse between the source and the drain. The large positive voltage at the control gate establishes an electric field in the oxide between the floating gate and the channel. This electric field attracts the hot electrons from the channel, generated by avalanche breakdown of the cell which is triggered by high drain and gate potentials. Electrons are further accelerated through the oxide and finally reach the floating gate. Charge stored at the floating gate is used to maintain a logical state.

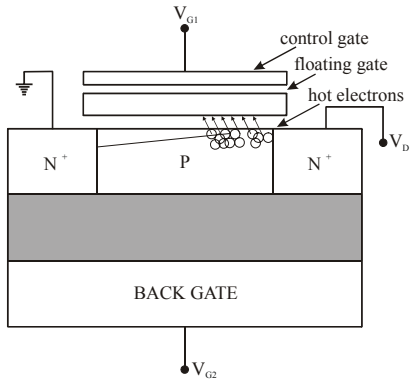

Fig. 1. Writing information into a SOI memory cell.

In a majority of EEPROM devices FN tunneling of carriers from the floating gate is used to erase information from it. In addition to the large dispersion of threshold voltage, this erase method is characterized by slow speed (compared to writing) and possible interface degradation [7,11]. The design of flash memory arrays suggested in this paper uses SOI cells which utilize a novel erase

method. This so called back-channel based erasure makes use of the SOI device back-gate and back-channel. Back control gate and drain are used to invert the back-channel and operate it in the avalanche breakdown state, so as to produce hot electron/hole pairs. Most of the generated electrons flow into the drain, while some are injected into the back (buried) oxide. The holes, on the other hand, are accelerated toward the floating gate and injected into it, as shown in Fig. 2. This erase method provides a tight threshold voltage distribution and a higher erase speed compared to bulk memory cells [12].

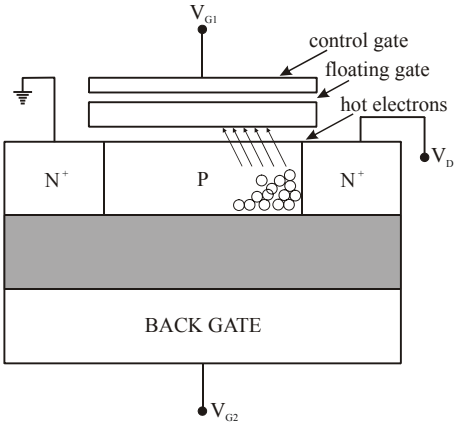

Fig. 2. Erasing information from a SOI memory cell.

3. Flash memory array layout and operation

An example of a flash memory array obtained using SOI memory cells is shown in Fig. 3. This array was designed in CMOS technology, using MAGIC VLSI Design Layout System. The diagram consists of the decoder, input/output logic, SOI memory cells and switch logic. The decoder is used to select a desired memory location to which the information is to be written, or from which it is to be read or erased. Switch logic (the SL blocks in Fig. 3) decides whether the voltage applied to the gates of SOI cells (transistors $T_{i\text{-}j}$ in Fig. 3, with $i = \overline{0,15}$, $j = \overline{0,15}$ for a 16x16 memory chip) is positive (+5 V) or negative (–5 V). The control signal (SL) has a low value (logic "0") when information is to be erased, and a high value (logic "1") when information is to be written or read. Input logic consists of a NAND/AND circuit with three input signals and a PMOS transistor. NAND/AND circuit input signals are Write (W), SL and Input Data (D_{INi}, $i = \overline{0,15}$). Output of the NAND/AND circuit $GP_i = \overline{D_{INi} \cdot W} \cdot SL$ is fed to the gate of the PMOS transistor. Output logic (lower part of Fig. 3) uses an NMOS pass transistor, which is controlled by the Read signal (R).

Details of the switch logic (SL) block from Fig. 3 are illustrated in Fig. 4. The switch logic consists of two parts, one for the write/read operation and another for erasing. These two parts are selected by the SL signal: SL = 1 during write/read operation, while during erase SL = 0.

When a specific address is selected, high voltage appers on the DEC line of the appropriate switch logic (Fig. 4). If either write or read is the desired operation, signal SL is set to 1 and the upper portion of the switch logic is on. Output of the second CMOS inverter is high (logic "1") and the gates of flash memory cells which are part of the selected word are brought to a high voltage level.

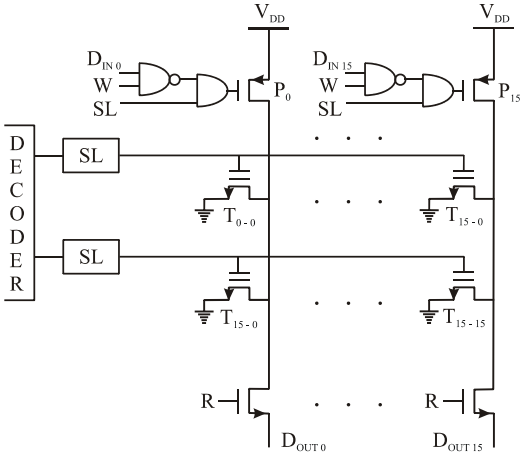

Fig. 3. Design of a memory array including input/output logic.

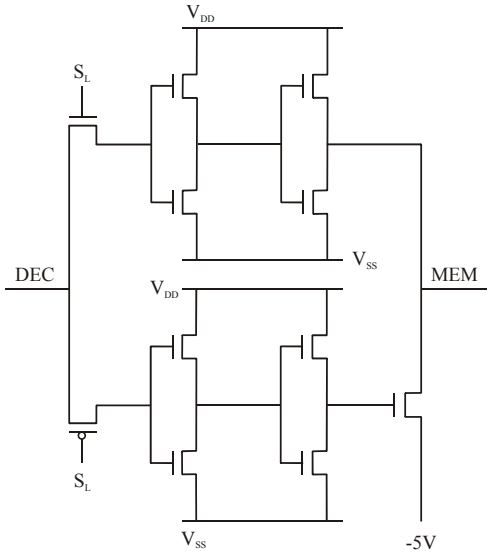

Fig. 4. Switch logic for controling the write/read and erase operations.

For writing information into memory cells, the write signal needs to be high (W = 1), while SL = 1. Signals D_{INi} are either "0" or "1", depending on the information being written. If $D_{INk} = 1$, gate voltage of the *k*-th PMOS is low (–5 V) and the transistor is on. This passes a high voltage to the drains of the corresponding SOI cells

(transistors T_{i-j} in Fig. 3, with $i = k$ and $j = \overline{0,15}$). In the SOI cell belonging to the *k*-th column which also belongs to the memory word selected by switch logic output, hot electrons from the channel are stored on the floating gate and the logic "1" is written. If $D_{INk} = 0$, gate voltage of the *k*-th PMOS is high (+5 V), the transistor is off and the drain voltage of SOI memory cells in the *k*-th column is zero, so the logic "0" is written into the cell belonging to the memory word selected by switch logic output. During the write operation signal R = 0 and the NMOS pass transistors are all off.

In case of the read operation W = 0 and SL = 1, so all PMOS transistors are turned off and the drain voltage of all SOI memory cells equals zero. Charge stored at the floating gate of a SOI cell with the logic "1" written into it makes its threshold voltage lower. Such a cell turns on when addressed by the switch logic, even with zero drain voltage. Cells with logic "0" written into them stay off when addressed at readout. Since for the read operation R = 1, information stored in the SOI cells belonging to the addressed word appears at D_{OUTi} outputs.

For performing the erase operation SL signal is set to low voltage (logic "0") and the lower portion of the switch logic is on (Fig. 4). Output of the switch logic is a logic "0" and the gates of SOI cells which are part of the selected word are brought to a low voltage level (–5 V). Since SL = 0, the gate voltage of all PMOS transistors is low (–5 V) and the transistors are on. The drain voltage of all SOI memory cells is high, and the ones belonging to the word addressed by the switch logic are erased through back-channel hole injection [11,13].

4. Conclusions

One way of designing a flash memory array is illustrated in this paper. It is a basic design of a 16×16 cell chip, using SOI cells utilizing a novel erase method based on the injection of hot holes from the back-channel to the floating gate. As described in the paper, an additional negative voltage level at the switch logic output is necessary to achieve this. SOI cell used for the design in this paper have only one control gate, which makes the inclusion of the program/erase switch circuitry necessary. If the cells were made with two control gates (one for programming and another for erasing) these switches could be eliminated. Additional circuitry could provide the possibility of blocking i.e. dividing the flash memory into individually erasable segments.

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