Dielectric constant of nano porous silicon at low frequencies under reverse bias by a standard experimental model

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Dielectric properties of layered structures of Gold/Porous Silicon/Silicon (Au/PS/Si) have been studied by applying alternating (AC) reverse bias voltages at low frequencies and at constant temperatures. The impedance measurements were carried out from 1 to 100 kHz, at room temperature when 20 mV AC reverse bias voltage was applied. The capacitance behavior of the structures was modeled in series combination by a standard equivalent circuit of two parallel RC networks. From the detailed analysis of the Au/PS/Si junction, the capacitance of the junction is calculated by using carrier concentration (N_A) and depletion layer width (W) values. It is found that, the capacitance of Au/PS/Si structure is mainly due to PS. The aim of this work is to study the influence of etching time and the effect of frequency change on the dielectric properties and the DC conductivity of the PS. The PS dielectric constant decreases as the etching time decreases and the frequency increases. Our results confirm that there is a relationship between the dielectric constant and frequency and the relationship can be stated as $\varepsilon \sim \omega^{-1}$.

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1. Introduction

Semiconductors are used widely in integrated circuits (IC) for electronic applications such as high speed computers and wireless communications. In these circuits, any single semiconductor microprocessor may have many transistors and transistor connection lines. As semiconductor geometries become smaller and smaller, some unwanted effects such as cross-talk, RC effects between neighboring metal lines and energy loss among lines arise in fabrication of these devices [1-4]. Therefore, a method for forming a material with reduced interlayer effects between is needed.

However, according to the Semiconductor Industry Association (SIA) roadmap an ultra-low dielectric constant material (material with a dielectric constant of 2.0 or less) is required for use in some nanometer integrated circuits. Therefore, significant amount of efforts have been made to use materials with low dielectric constants in those integrated circuits. One of the important materials is porous silicon (PS) which has dielectric constant from 1.3 to 4. Low dielectric constant of PS comes from its highly porous structure [5-6]. PS as a connection line has a low dielectric constant and is stable even at temperatures higher than 900 ˚C.

PS is a material that is made out of a p-type or n-type silicon wafer by a chemical process or electrochemical anodization etching. Etching electrolyte is usually a solution of HF, ethanol, and H_2O with different concentrations. Electrolyte concentration, current density, and etching time are the variables that characterize the properties of PS layers and they determine the porosity, shape, and pore height in PS [7]. Measurement of PS capacitance is one of the useful experimental attempts for studying the electrical properties of PS layers. Measurement of AC reverse bias voltage is an important way for dielectric characterization of materials. The dielectric analysis is interpreted in term of impedance measurement and usually has been shown by an equivalent circuit that is formed by a RC network [3]. AC impedance and dielectric constant measurements of PS show that it's conductivity strongly depends on frequency and this dependence obeys a universal scaling (it varies from $\omega^{½}$ to ω) which is governed by fractal properties of PS [8-9].

In the present work, etching time is varied to observe change in the morphology of PS samples. Also, we calculate capacitance and dielectric constant of PS samples; measured in the low frequency range of 1 kHz to 100 kHz by a convenient circuit.

2. Experimental

PS samples were obtained from (100) oriented p-type silicon wafers with resistivity of 0.2-0.5 Ω cm. Before anodization, 500 nm Al ohmic layer was evaporated on the backside of the wafers followed by annealing process at 400 ºC for 40 minutes. A thin wire was attached to back side of samples by silver paint and then the back side of the samples was covered by an acid proof wax. The electrochemical anodization of Si wafers was carried out using in a two-electrode electrolytic cell with the Si as the

working electrode and Pt sheet as the counter electrode under constant current at room temperature. Anodization current density was kept at 30 mA/cm^2. The electrolyte was an ethanol (Merck) and 48% HF (Merk) with volume ratio of (1:10). The structure and morphology of PS could be controlled by adjusting the etching time from 10- 40 min. Our samples were made in day light and at room temperature.

Characteristics of PS samples are explained in Table 1. SEM images of prepared samples are shown in Fig. 1. For achieving Au/PS/Si structure, PS samples are coated with 20 nm thin Au layers using a thermal vacuum evaporation system (Sputter Coater System, model SCD001).

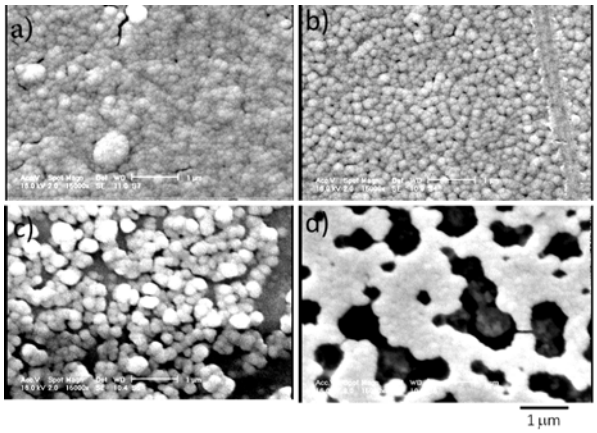

Fig. 1. Top view SEM images of (a) PS1, (b) PS2, (c) PS3, and (d) PS4.

Table 1. Anodization parameters for preparation of PS samples.

Sample	Current density (mA/cm^2)	Etching time (min)	Thickness (µm)	Porosity (%)
PS1	25	10	10.6	60
PS2	25	20	22.2	70
PS3	25	30	26.9	78
PS4	25	40	38.8	84

Thickness (L_{PS}) and porosity (P) of PS samples are calculated by a gravimetric method [15]. L_{PS} and P can be calculated by the following equations:

$$L_{PS} = (m_1 - m_3)/(\rho\, s)$$

$$P = (m_1 - m_2)/(m_1 - m_3) \quad (1)$$

where m_1 is sample mass before anodization, m_2 is sample mass after anodization, m_3 is sample mass exactly after rapid dissolve the PS layer into 3% KOH solution, s is sample surface area, and ρ is Si density (= 2.33 gr/cm^3) [16-17].

Dielectric capacitance measurements were done by a simple circuit that is shown in Fig. 2. A function generator applies an AC voltage (20 mV) between the two electrodes at a frequency in the range of 100 Hz. In each frequency, current is measured by an Escort 3146A model multi meter. Frequency and voltage also are measured simultaneously by another Escort 3146A model multi meter.

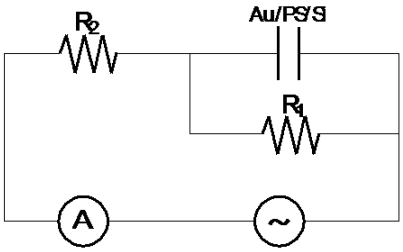

Fig. 2. Designed circuit for capacitance measurement of Au/PS/Si. Voltmeter measures total voltage (V_T), PS voltage (V_{PS}), and resistance voltage (V_R) in circuit (a), (b), and (c) respectively.

3. Results and discussion

As Fig. 1 shows, the PS samples generally contain interconnected pores that pores diameter increase with a weak dependence on etching time and have an average diameter of less than 50 nm. However, the rise of etching time results in increase of the porosity. To calculate the dielectric constants of the PS structures an electronic circuitry (equivalent circuit shown in Fig. 3) can be proposed and related brief explanation of the principle is as following; If a parallel plate capacitor is subject to an alternating voltage of $V = V_0 \cos\omega t$ in a circuit, the plates of the capacitor are going to be charged with positive and negative charges alternatively. So, electrical charges in the circuitry move from one plate to the other plate generating an alternative current with a certain frequency. An equivalent circuit, two parallel RC networks with R_s and L, for PS structure is proposed in Fig. 3.

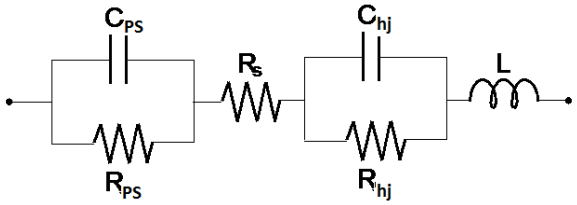

Fig. 3. Equivalent circuit has been used for equivalent impedance measurement.

According to Fig. 3, the circuit includes a parallel resistance R_{hj} and a capacitor C_{hj} that show resistance and capacitance of a Au/PS/Si heterostructure, an inductor L which represents self-induction and a resistance R_s which is coming from existing wires in the circuit. In the circuit, parallel resistance R_{PS} and capacitor C_{PS} show resistance and capacitance of a PS sample respectively. Equivalent impedance of the circuit shown in Fig. 3 can be formulated as following [18]:

$$Z_{eq}(\omega) = R_S + \frac{R_{PS}}{(iC_{PS}R_{PS}\omega + 1)} + \frac{R_{hj}}{(iC_{hj}R_{hj}\omega + 1)} + i\omega L \tag{2}$$

where ω is angular frequency of AC signal. Equivalent impedance of Eq. 2 can be represented in its real and imaginary components. So, for the used values of C_{PS}, C_{hj}, R_{PS}, R_{hj} in frequencies lower than 1 MHz we can ignore series resistance R_s and insulator L effects [20].

Therefore, total capacitance (C_T) of Au/PS/Si can be modeled as series combination of PS layer capacitance (C_{PS}) and PS/Si heterostructure capacitance (C_{hj}). PS/Si junction is similar to a p-n junction due to difference between PS and Si band gaps. Therefore, capacitance of PS/Si heterostructure (C_{hj}) can be calculated similar to capacitance of p-n junction. Then it will be

$$C_{hj} = A\sqrt{\frac{\varepsilon_{Si}\varepsilon_0 eN_A}{2\Psi_s}} \quad ;$$

$$\begin{cases} \Psi_s = V_T - V_{PS} \\ N_A = 5\times10^{17}\, cm^{-3} \\ \varepsilon_{Si} = 11.9 \\ \varepsilon_0 = 8.85\times10^{-12}\,\dfrac{F}{m} \end{cases} \quad \Rightarrow \quad C_{hj} \approx 10^{-5}\, F \tag{3}$$

where V_T is total applied voltage to the circuit and V_{PS} is measured voltage for the capacitor including PS dielectric (Fig. 2). C_{hj} determines from Eq. 3 in lower frequencies and is in order of 10^{-5} F. Also experimental measurements of capacitances of PSs are found to be in the order of 10^{-9} F. Therefore C_{hj} is negligible in Eq. 4 and total capacitance (C_T) can be equal to PS capacitance [19].

$$\frac{1}{C} = \frac{1}{C_{PS}} + \frac{1}{C_{hj}} \tag{4}$$

Then by assuming above mentioned conditions, Au/PS/Si equivalent circuit can be given with a circuit that has only the Au/PS/Si capacitor parallel to PS resistance. By using fig. 2 circuits (which are designed for the measurement of PS total capacitance), PS resistance (R_{PS}) and PS capacitance (C_{PS}) can be measured. Total voltage (V_T), PS capacitor voltage (V_{PS}), R_2 voltage (V_{R2}), and variation of current versus applied frequency are measureable by using the circuits in Fig. 2. Parallel resistance R_1 (about 10^4 Ω) and series resistance R_2 (about 10^3 Ω) are used in the Fig. 2 circuits for reduction of PS equivalent resistance (about 10^4-10^6 Ω) and for calculating the PS capacitance and resistance.

Current variations versus the frequencies for the PS samples are measured by using the circuits in Fig. 2. Then, PS capacitance and resistance can be obtained by the following equations:

$$V_T = I_T\left|Z(\omega)\right| \tag{5}$$

$$\left|Z(\omega)\right| = R_2 + \frac{R}{\sqrt{1+C^2\omega^2R^2}} \tag{6}$$

R in Eq. 6 is an equivalent resistance between PS resistance (R_{PS}) and R_1, so it is equal to $R = \dfrac{R_{PS}R_1}{R_{PS}+R_1}$.

Also the loss angle (δ) can be measured by measuring total voltage (V_T), capacitance voltage (V_C), and R_2 voltage (V_{R2}) with the following relations:

$$\cos\delta = \frac{V_T^2 - V_{R_2}^2 - V_C^2}{2V_{R_2}V_C} \tag{7}$$

At last, using the following equations:

$$\tan\delta = \frac{\mathrm{Im}(Z)}{\mathrm{Re}(Z)} \tag{8}$$

$$\tan\delta = -\frac{\omega CR^2}{R_2 + R + \omega^2C^2R^2R_2} \tag{9}$$

PS resistance and dielectric capacitance in terms of applied frequencies has been obtained. The behavior of real and imaginary parts of dielectric constants of the PS samples is connected to PS capacitance by the following relations [20].

$$\varepsilon'_{PS}(\omega) = C(\omega)\frac{L_{PS}}{A} \tag{10}$$

$$\varepsilon''_{PS}(\omega) = \varepsilon'_{PS}(\omega)\tan\delta \tag{11}$$

where A is junction area and L_{PS} is PS thickness and ε'_{ps} and ε''_{ps} are real and imaginary parts of dielectric constant of PS, respectively. ε'_{ps} and ε''_{ps} versus frequency are shown in Fig. 4 and Fig. 5, respectively. As the figures shows, dielectric constants of PS decrease with increasing the frequency. It is concluded that this is connected to PS transport mechanism [21]. At room temperature, PS dielectric behavior can be explained by low frequency (LF) and high frequency (HF) reduction procedures. The LF procedure was assigned to a transport of charged carriers across the disordered fractal structure of PS. But at higher frequencies the distance taken by the carriers before the electric field changes its polarity is shorter than the fractal length scale and a shorter length scale is responsible for the transport of the carriers. Effect of LF reduction procedure becomes smaller quickly during the first oxidation stage and disappears after 30 sec of the oxidation. In contrast, HF procedure resists oxidizing until second oxidation stage [21]. Since our PS samples can be

oxidized after preparation and as figs 4 and 5 show, it can be claimed that the samples' dielectric responses follow the HF transportation mechanism.

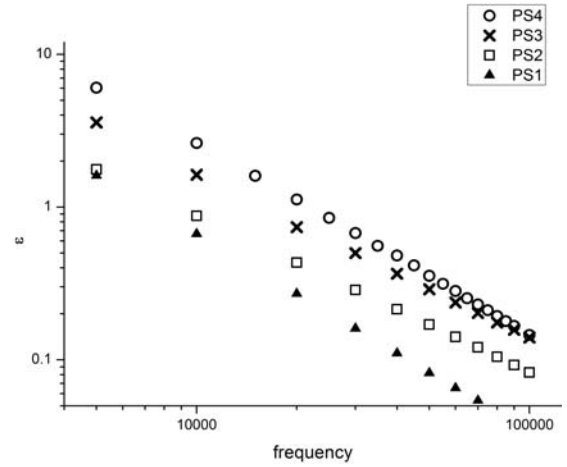

Fig. 4. Real part of PS dielectric constant versus frequency for four different etching times.

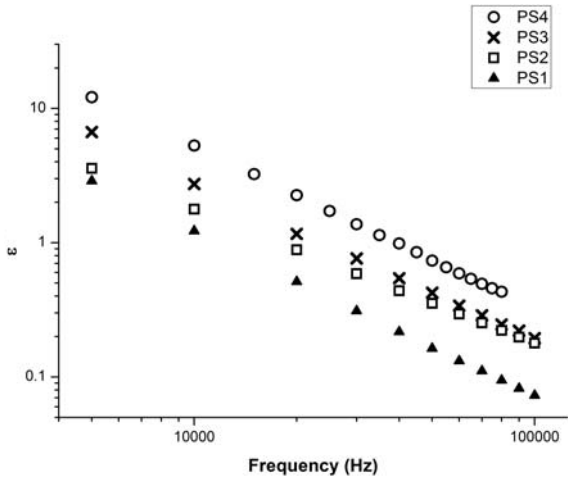

Fig. 5. Imaginary part of PS dielectric constant versus frequency for four different etching times.

According to proposed model by Ben-chorin [7] and Ballberg [22], the HF transport was assigned to a transport of charged carriers between the silicon nanocrystals. On the other hand, this transportation channel is related associated with the hopping between silicon nanocrystals in the PS samples and the oxidation do not affect this intercrystalline transport [23]. By using Kramers-Kronig relations, we can show that for this transportation channel, the dielectric function should behave as $\varepsilon \sim \omega^{-1}$.

The dependence of PS dielectric constant on the sample thickness (reported in table 1) is shown in fig. 6. As the figure shows the dielectric constant increases by increasing the PS thickness. This result is in contrast to the fact that by increasing the etching time and the PS thickness, the dielectric constant should decrease due to development of pores in the silicon layer. However, our SEM images showed that an inhomogeneous porous structure and a sponge-like structure were formed on our samples, so this inhomogeneity produces a high surface area. It is note that the porosity may consist of: *(i)* open porosity where the pores are interconnected; *(ii)* closed porosity where the pores are isolated and not interconnected; and *(iii)* through-porosity where the pore extends through the surface to the interface. Open porosity may be of several forms. Uniformly distributed interconnected pores develop as the pore volume becomes large (greater than about 5%). Open porosity can affect material properties including: (i) high surface areas; (ii) easy access to the interfacial region; and (iii) easily deformed material [24-26]. So, we claim that our porosity consists of open porosity and its undesirable effects got high surface area. Therefore, the dielectric constant increases by increasing the etching time and PS thickness.

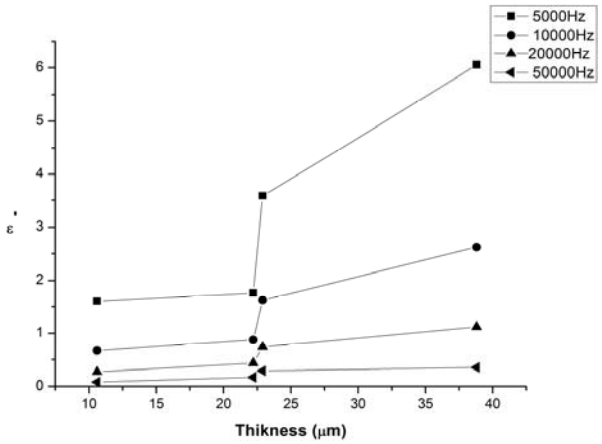

Fig. 6. Real part of PS dielectric constant versus the thickness for four different applied frequencies.

Dielectric constant of PS varies with etching time as shown in Figs. 4 and 5. Therefore, PS samples can be made for particular applications in order to obtain desired dielectric capacitance by controlling anodization parameters.

With obtained capacitance and dielectric constants of PS, we can find physical and microstructure characteristics of PS such as thickness, porosity, surface area, and refractive index. Here, only dc conductivity and complex refractive indexes of PS samples are calculated by using PS capacitance and dielectric constants.

By using Kramers-Kronig relation between the real and imaginary parts of dielectric constant and dc conductivity, Eq. 12, the dc conductivity versus applied frequencies can be found (Fig. 7).

$$\frac{\sigma_{dc}}{\omega} = \varepsilon''(\omega) + \frac{2\omega}{\pi} P\int_0^{\infty} \frac{\varepsilon'(\omega')d\omega'}{\omega'^2 - \omega^2} \qquad (12)$$

As fig. 7 shows, by increasing the applied frequency dc conductivity shows a slightly change for all the PS samples.

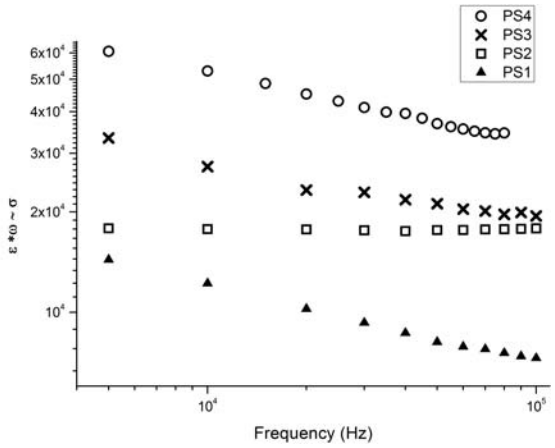

Fig. 7. DC conductivity of PS samples versus frequency for four different etching times.

Real and imaginary parts of PS complex refractive index can be calculated in terms of real and imaginary parts of PS dielectric constant by using following relations:

$$n = [\frac{1}{2}(\varepsilon' + \sqrt{\varepsilon'^2 + \varepsilon''^2})]^{1/2} \quad (13)$$

$$k = [\frac{1}{2}(-\varepsilon' + \sqrt{\varepsilon'^2 + \varepsilon''^2})]^{1/2} \quad (14)$$

Fig. 8 (a) and (b) show PS refractive index (real part) and PS extinction coefficient (imaginary part) for four different etching times, respectively. Imaginary part of complex refractive index shows direct relation with absorption. In general, when the absorption of a layer cannot be negligible, k is non zero. Then by drawing k versus energy (E = ħω) graph, we can show the absorption region of PS layer. Fig. 8 (b) confirms that PS absorption is reduced by increasing energy for all the samples.

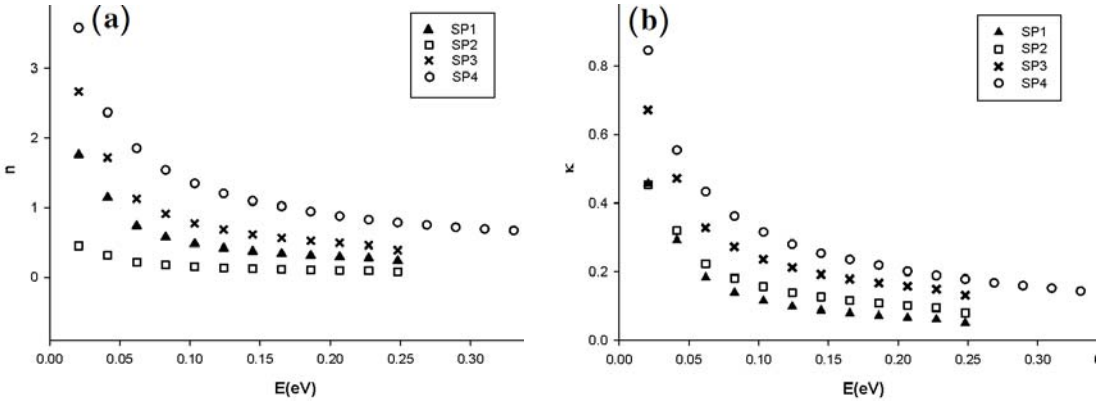

Fig. 8. (a) Real part and (b) imaginary part of PS complex refractive index for four different etching times respectively.

4. Conclusion

PS includes a network of nanometer sized of nanocrystal silicon zones that are surrounded by voids. The nano PS samples were prepared with electrochemical method. Samples with different porosity and thickness were obtained by controlling etching time as an important and effective anodization parameter. Low dielectric constant can be obtained due to highly porous structure of PS. The dielectric constant of PS samples as a function of frequency is measured by a simple electrical circuit.

The behavior dielectric constants of the PS samples as a function of frequency show $\varepsilon \sim \omega^{-1}$ relationship. This behavior confirms predictions of the transportation theory in irregular PS geometry related to intercrystallites transport at high frequencies. DC conductivity, real and imaginary parts of PS refractive index as a function of frequency are also calculated.

Acknowledgment

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