Electrical characteristics and interfacial reactions of rapidly annealed double metal Pd/Ti Schottky structure on n-type InP

M. BHASKAR REDDY[a], V. RAJAGOPAL REDDY[b,*], D. SUBBA REDDY, CHEL-JONG CHOI [b]
Department of Physics, Sri Venkateswara University, Tirupati 517 502, India
[a]*Government Degree College, Department of Physics, Puttur-517583 Chittor Dt. A.P., India*
[b]*School of Semiconductor and Chemical Engineering, Semiconductor Physics Research Center (SPRC), Chonbuk National University, Jeonju 561-756, Korea.*

We report on the effect of annealing temperature on electrical, interfacial reactions and surface morphological properties of Pd/Ti Schottky contacts to n-type InP. Measurements showed that the Schottky barrier height of as-deposited Pd/Ti Schottky contact is 0.58 eV (I-V) and 0.79 eV (C-V) respectively. It is observed that the barrier height increases to 0.67 eV (I-V) and 0.87 eV (C-V) for the contact annealed at 250 ^{o}C. Experimental results show that after annealing at temperature of 350 ^{o}C and 450 ^{o}C, the barrier heights decreases to 0.60 eV (I-V), 0.82 eV (C-V) and 0.54 eV (I-V), 0.73 eV (C-V) respectively. From the above observations, the optimum annealing temperature for the Pd/Ti Schottky contact is 250 ^{o}C. Based on the AES and XRD analysis, the formation of the indium phases at the Pd/Ti/n-InP interface could be the reason for the increase in the barrier height at annealing temperature 250 ^{o}C. Further, the degradation of the barrier heights after annealing at 350 ^{o}C and 450 ^{o}C may be due to the formation of phosphide phases at the Pd/Ti/n-InP interface. Atomic force microscopy (AFM) result shows that the overall surface morphology of the Pd/Ti Schottky contacts is reasonably smooth.

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1. Introduction

In recent years, group III-V semiconductors have drawn considerable attention since they are technologically important as their electronic properties can be varied easily with different dopants [1]. It also has a higher mobility, with a high peak-to-valley ratio in the velocity electric-field characteristics. These qualities are essential for high-speed microwave field-effect transistors, transferred electron oscillators and high-speed logics. The energy gap of InP is close to the optimum value for efficient conversion of solar radiation into electric power by single-junction photovoltaic cells [2]. Metal-semiconductor (MS) structures play an important role in the device based on the III-V compound semiconductors in the form of Schottky barrier diodes (or) ohmic contacts [3]. The fabrication of reliable and well-controlled electrical contacts is the key to the successful operation of almost all solid-state semiconductor devices. The continuous scaling of microelectronic devices to sub-microelectronic dimensions increases the need for high performance and rectified contacts [4]. Many investigations have been undertaken in order to improve the electrical behaviour of the contact (decrease of leakage current, an increase of barrier height), which strongly depends on the semiconductor surface preparation and on the metal used for Schottky contact. The surface Fermi level pinning that arises from the high density of surface states and other nonstoichiometric defects, make it difficult for n-InP to obtain a Schottky barrier height (SBH) greater than 0.5 eV [5,6]. Such a low barrier height causes a large reverse leakage current and bad electrical performance for Schottky diodes made of n-InP. Therefore, the formation of a high Schottky barrier height is an important research issue in InP device development.

Efforts have been made to improve Schottky barrier heights by several research groups [7-19]. For example, Chen *et al* [10] fabricated Pd Schottky contact on n-InP, reported that the Schottky barrier height lowered and ideality factor increased with the increase of the hydrogen concentration. Horvath *et al* [11] prepared Au/n-InP Schottky diode and found that the best Schottky barrier height of 0.83 eV was achieved using HCL:H_2O surface treatment. Cetin *et al* [12] fabricated Au, Al and Cu/n-InP (100) Schottky barrier diodes on n-InP surface and investigated the influence of the air-grown oxide on the electrical performance. Janardhanam *et al* [13] studied the effect of rapid thermal annealing on the electrical and structural properties of Ru/n-InP (100) Schottky rectifiers. They reported that the increase in barrier height after annealing at 500 ^{o}C might be due to the formation of indium phases at the interface. Bhaskar Reddy *et al* [14] investigated the effects of thermal annealing temperature on the electrical and structural properties of Pd/Au Schottky contacts to n-InP and reported that the Schottky barrier height was 0.51 eV (I-V) and 0.92 eV (C-V) for the contact annealed at 400 ^{o}C. Gullu [15] studied the ultra high (100%) barrier modification of n-InP Schottky diode

by DNA biopolymer nano films, reported that the DNA increases an effective barrier height as high as 0.87 eV by influencing the space charge region of n-InP device. Soylu *et al* [16] investigated the effects of annealing on Au/pyronine–B/MD/n-InP Schottky diode and reported that the barrier height and ideality factors were 0.60 eV and 1.041, 0.57 eV and 1.253 after annealing at 100 and 250 ^{o}C. Cetin *et al* [17] prepared Au and Cu Schottky contacts on n-InP and found that the effective barrier height of the Au and Cu Schottky contacts was 0.480 eV, 0.404 eV and 0.524 eV, 0.453 eV from I-V and C-V measurements. Ucar *et al* [18] studied the effect of hydrostatic pressure on the electrical properties of Au/n-InP Schottky diodes. They reported that the barrier height and ideality factor of Au/n-InP diodes were in the range of 0.546-0.579 eV and 2.36-1.93 for the 0.0-5.0 kbar pressure interval at room temperature. Recently Bhaskar Reddy *et al* [19] studied the influence of rapid thermal annealing on electrical and structural properties of double metal structure Au/Ni/n-InP diodes. They found that the as-deposited Au/Ni Schottky contacts exhibited high barrier height and low reverse leakage current than the annealed contacts.

The main aim of the present work is to fabricate double metal structure Pd/Ti Schottky contacts on n-type InP and investigate its electrical, structural and surface morphological properties. To the best of our knowledge, Pd/Ti metal scheme has not been explored as Schottky contacts on n-type InP. In this work, titanium (Ti) is selected as a first contact layer because it has low work function and it provides the lowest forward voltage drop as well. The transition metal palladium (Pd) is used as a second contact layer because it has high metal work function, high reliability and it reacts with InP. There is a serious lack of information about the effect of rapid thermal annealing (RTA) on the electrical characteristic of near noble metal/InP Schottky contacts. Generally devices are subjected to annealing in the processing of integrated circuits. From a device point of view, it is important to know what happens to metal contacts on InP when they are annealed. Therefore, we made an attempt to investigate the change in the electrical, interfacial reactions and surface morphological properties of Pd/Ti/n-InP Schottky diodes as a function of annealing temperature.

2. Experimental details

In the present work, Pd/Ti/n-InP Schottky diodes were prepared on cleaned n-type InP wafer which was grown by Liquid Encapsulated Czochralski (LEC) technique. The carrier concentration determined by means of Hall measurements was about 5.0×10^{15} cm^{-3}. Before making the ohmic contact, the samples were initially degreased with warm organic solvents like trichloroethylene, acetone and methanol by means of ultrasonic agitation in sequence of 5 min in each step to remove the undesirable impurities and followed by rinsing in deionized (DI) water. The samples were then etched with HF (49 %) and H_2O (1:10) to remove the native oxides from the substrate. The wafer was then dried with high-purity nitrogen and inserted into the deposition chamber immediately after the etching process. Ohmic contacts of thickness 700 A□ were formed with indium on the rough side of the InP wafer under a pressure of 7×10^{-6} mbar. Then, the low resistance ohmic contact for n-InP was achieved by thermal annealing at 350 ^{o}C for 1 min in flowing nitrogen atmosphere in a rapid thermal annealing (RTA) system. Pd/Ti (30 nm/30 nm) Schottky contacts were fabricated on n-InP using stainless steel circular mask of diameter of 0.7 mm on the polished side of n-InP wafer using electron beam evaporation, the InP material was screened from the electrons originally at the filament of the electron beam evaporator [20]. The metal layer thickness and the deposition rates were monitored with the help of a digital crystal thickness monitor. The Pd/Ti Schottky contacts were rapidly annealed in the temperature range of 150 ^{o}C – 450 ^{o}C for duration of 1 min in nitrogen atmosphere. The current – voltage (I-V) and capacitance-voltage (C-V) characteristics of Pd/Ti Schottky contacts were measured using Keithley source measuring unit (Model No. 2400) and automated DLTS (DLS-83 D) system at room temperature. Auger electron spectroscopy (AES: UG: Micro lab 350) depth profile was performed to examine the intermixing of the metal and InP before and after annealing. X-ray diffraction (Siefert, XRD PW 3710, λ=1.54 Å.) using CuKα radiation was employed to characterize the interfacial reactions between the metals and InP layers. Using atomic force microscopy (AFM) (make and model no.: Nano Focus, MOD-1M Plus, operating mode: non-contact mode, tip size<10nm), the surface morphology of the Pd/Ti Schottky contacts were assessed before and after annealing temperature.

3. Results and discussion

3.1 Current-voltage (I-V) and capacitance-voltage (C-V) characteristics

The Pd/Ti Schottky diodes have been evaluated using measurements of forward and reverse I-V and C-V characteristics at room temperature. The thermionic emission theory for charge transport in Schottky structures is used to analyze the data. When a nearly ideal Schottky barrier diode (SBD) is considered, it is assumed that the forward bias current of the device is due to thermionic emission (TE) current and it can be expressed as [5]

$$I = I_o \exp\left(\frac{qV}{nkT}\right)\left[1-\exp\left(\frac{-qV}{kT}\right)\right] \qquad (1)$$

where

$$I_0 = AA^{**}T^2 \exp\left(\frac{-q\phi_{eff}}{kT}\right) \qquad (2)$$

here I_o is the saturation current, ϕ_{eff} is the zero bias effective barrier height, A^{**} is the effective Richardson constant and is equal to 9.4 Acm^{-2}k^{-2} for n-type InP, [21] A

is the diode area, n is an ideality factor, q is the electron charge, k is the Boltzmann's constant and T is the absolute temperature. Fig. 1 shows the typical current-voltage (I-V) characteristics of Pd/Ti Schottky contacts to n-type InP as a function of annealing temperature. For the as-deposited Pd/Ti Schottky contact, the leakage current is found to be 1.87×10^{-5} A at -1 V. For the contacts annealed at temperatures 150 °C, 250 °C, 350 °C and 450 °C, the corresponding leakage currents are 1.66×10^{-5} A, 4.83×10^{-7} A, 3.85×10^{-6} A and 2.69×10^{-5} A at -1 V, respectively. It is noted that the leakage current decreases for the contact annealed at 250 °C compared to the as-deposited contact. However, it is observed that the leakage current slightly increases upon annealing at temperature 450 °C. Calculations showed that the SBH is 0.58 eV for the as-deposited contact and for annealed samples 0.59 eV at 150 °C, 0.67 eV at 250 °C, 0.60 eV at 350 °C and 0.54 eV at 450 °C. From the above observations, it is observed that the maximum barrier height is 0.67 eV for the contact annealed at 250 °C. Therefore, the optimum temperature for the Pd/Ti Schottky contact is 250 °C.

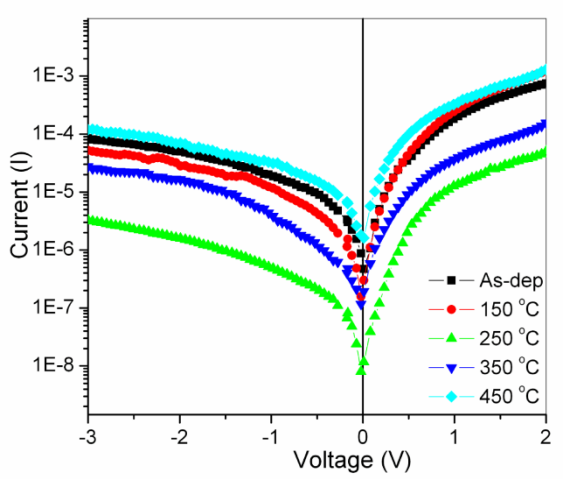

Fig. 1.Typical I-V characteristics of Pd/Ti Schottky contacts to n-InP as a function of annealing temperature

The ideality factor n is a measure of conformity of the diode to pure thermionic emission and if n is equal to one, pure thermionic emission occurs. However, n has usually a value greater than unity. It is extracted from the slope of the straight line region of the forward bias ln I-V characteristics through the relation

$$n = \frac{q}{kT}\frac{dV}{d(\ln I)} \tag{3}$$

The ideality factor of Pd/Ti Schottky contact is found to be 1.46 for the as-deposited contact. The ideality factor is improved to 1.18 upon annealing at 250 °C for 1 min in nitrogen ambient. The values of ideality factors are indicative of non-ideal behaviour, suggesting the transport mechanism, other than just thermionic are probably present in these diodes. Our data clearly shows that the diodes have ideality factors that are larger than one. The higher values of ideality factor are probably due to the potential drop in the interface layer and the presence of excess current and the recombination current through the interfacial states between the semiconductor/insulator layers [22].

As an alternate method to conventional analysis, Norde method is also employed [23] to compare the Schottky barrier height of Pd/Ti Schottky contacts, since the high series resistance hinders the accurate evaluation of barrier height from standard ln (I)-V plot. In this method, a function F (V) is plotted against the V and is given by

$$F(V) = \frac{V}{2} - \frac{kT}{q}\ln\left[\frac{I(V)}{AA^{**}T^2}\right] \tag{4}$$

The effective SBH is given by

$$\phi_b = F(V_{\min}) + \frac{V_{\min}}{2} - \frac{kT}{q} \tag{5}$$

where $F(V_{min})$ is the minimum value of F(V) and V_{min} is the corresponding voltage. The V_{min} is obtained from the plot of F (V) versus V for the Pd/Ti Schottky contacts (figure not shown here). The extracted Schottky barrier heights of Pd/Ti contacts are 0.64 eV for the as-deposited contact, 0.61 eV, 0.70 eV, 0.63 eV and 0.59 eV for the contacts annealed at 150 °C, 250 °C, 350 °C and 450 °C. It is observed that these values are in good agreement with those obtained by the I-V method.

Capacitance measurement is one of the most important nondestructive methods for obtaining information on rectifying contact interfaces. In some contacts, the capacitance under forward bias is larger than the space-charge capacitance predicted by the basic theory. The difference between the measured and the space-charge capacitance is called the excess capacitance, and is attributed to interface states. The interface states can be created by crystal lattice discontinuities (dangling bonds), interdiffusion of atoms (or) a large density of crystal lattice defects close to the metal/semiconductor interface [5]. Capacitance-voltage (C-V) measurement is performed for as-deposited and annealed Pd/Ti Schottky contacts at a frequency of 1 MHz at room temperature. Fig. 2 shows the plot of $1/C^2$ as a function of bias voltage for as-deposited and contact annealed at different temperatures. The tangent to the C^{-2} versus V plot emerged essentially from a point in the voltage axis. The C^{-2} versus V plot showed that the capacitance C decreases less slowly with increasing applied bias, because deep-level traps are increasingly exposed by the inverse in the depletion region width which is caused by the reverse bias. The C-V relationship for Schottky diode is given by [24]

$$\frac{1}{C^2} = \left[\frac{2}{\varepsilon_s q N_d A^2}\right]\left[V_{bi} - \frac{kT}{q} - V\right] \tag{6}$$

where V_{bi} is the flat band voltage, N_d is the donor concentration, A is the area of the Schottky contact and ε_s is the permittivity of the semiconductor ($\varepsilon_s = 11\varepsilon_0$). The x-intercept of ($1/C^2$) versus V plot yields V_o, and V_o is related to the built in potential, $V_{bi} = V_0 + kT/q$, where T is absolute temperature. The barrier ϕ_{CV} is given by $\phi_{CV} = V_{bi} + V_n$, where $V_n = \left(\frac{kT}{q}\right)\ln\left(\frac{N_c}{N_d}\right)$. The density of states in the conduction band edge is given by $N_c = 2(2\Pi m^* kT/h^2),^{3/2}$ where $m^* = 0.078\ m_o$ and its value is 5.7×10^{17} cm^{-3} for InP [24] at room temperature. The estimated barrier heights of Pd/Ti Schottky contacts from C-V measurements are 0.79 eV for as-deposited, 0.80 eV for 150 °C, 0.87 eV for 250 °C, 0.82 eV for 350 °C and 0.73 eV for 450 °C respectively. The calculated carrier concentration of Pd/Ti Schottky contacts are 5.77×10^{15} cm^{-3} for the as-deposited, 4.67×10^{15} cm^{-3} and 6.39×10^{15} cm^{-3} for the contacts annealed at 250 °C and 450 °C. It is noted that the estimated carrier concentration values from C-V measurements are more (or) less than the values determined using Hall measurements. In C-V measurements, the net doping concentration is the difference of electrical active concentration of donors and acceptors. Since the Schottky contacts are leaky and the leakage current disturbs the capacitance measurements and consequently there may be an error in estimation of the doping concentration. This may be the reason for the carrier densities calculated from C-V to have slightly more (or) less value compared to the value measured from Hall measurements.

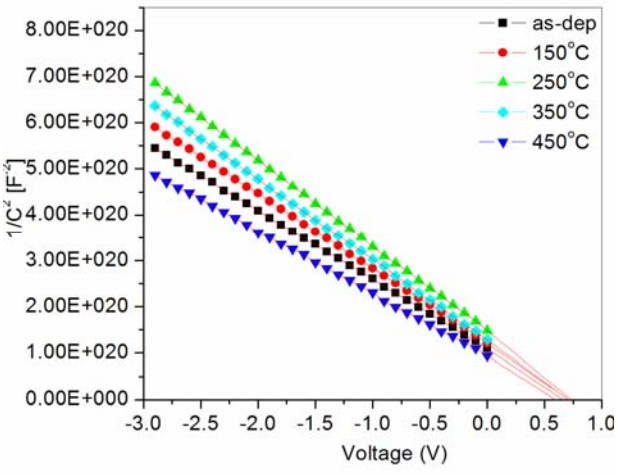

Fig. 2. Plot of $1/C^2$ versus V for Pd/Ti Schottky contacts to n-InP annealed at different temperature

The annealing temperature treatment also has a large effect on diode I-V characteristics. Fig. 3 shows a comparison of measured barrier height values, ideality factor values for Pd/Ti/n-InP diodes annealed for 1 min in nitrogen ambient at 150 °C, 250 °C, 350 °C and 450 °C. This clearly indicates that the 250 °C annealing contact gives the best result ($\phi_b = 0.67$ eV, n = 1.18) and also has the lowest reverse leakage current (4.83×10^{-7} A). However, when the contact annealed at 450 °C, the barrier height has significantly decreased to 0.54 eV and the ideality factor also has deteriorated. From Fig. 3, it is evident that the barrier height ϕ_b obtained from I-V measurements are lower than those obtained from C-V measurements. The difference in the barrier height from these methods may be due to inhomogeneity at the interface. This inhomogeneity results from the formation of non-uniform products of reaction at the interface at high temperatures and may vary from one location to another. Another possibility is that the interfacial capacitance and the capacitance due to depletion layer is in series, the total capacitance decreases and as a result C^{-2} increases. This increases the intercept of C^{-2} versus V plot, which gives the barrier height. As the I-V method involves the flow of electrons from semiconductor to metal, the barrier height determined from those methods will logically yield lower barrier heights (or) a combination of low and high barrier heights. This process is known as parallel (or) mixed-phase contact [25, 26]. Further, there are some general reasons which have mentioned in the literature, such as surface contamination at the interface, deep impurity levels, an intervening insulating layer, quantum-mechanical tunneling, image-force lowering and edge leakage currents [24, 27, 28].

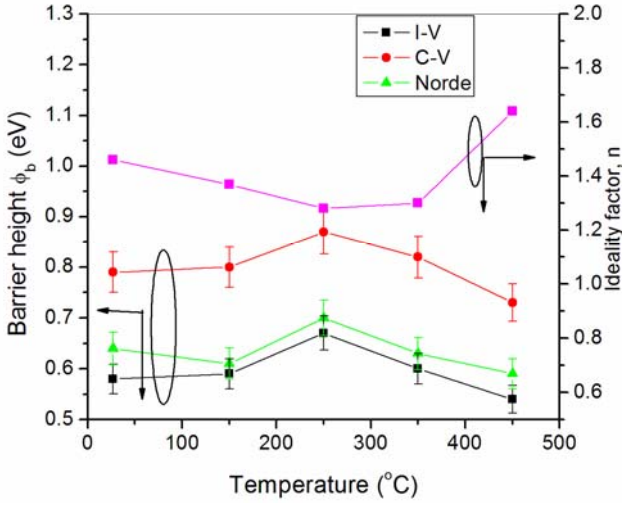

Fig. 3. Effective barrier height and ideality factor of Pd/Ti/n-InP diodes after annealing for 1 min at different temperature.

3.2 Structural and morphological characteristics

In order to investigate inter-diffusion between the metals and InP layers before and after annealing, the auger electron spectroscopy (AES) measurement is performed. The depth profiles of the Pd/Ti Schottky contacts on n-InP before and after annealing are shown in figure 4. Peak-to-peak intensities are recorded as a function of sputtering time and the results are discussed only in the qualitative way. For the as-deposited sample, the individual layers of Pd and Ti are well defined which indicate the absence of significant interfacial reaction between the metal layers and the InP are shown in Fig. 4(a). For the sample annealed at 250 °C, Fig. 4(b), it is observed that some amount of indium (In) is out-diffused into metal layers. This is indicative of possible reaction between Pd/Ti metal

layers and In, which would lead to the formation of Ti- and Pd-In interfacial phases at the interface during annealing process. However, a small amount of indium (In) is out-diffused further into the metal layers when the contact is annealed at 450 °C. In addition, a small amount of P is also out-diffused into the metal layers, indicating the formation of Pd- and Ti-P interfacial phases at the interface as shown in Fig. 4(c).

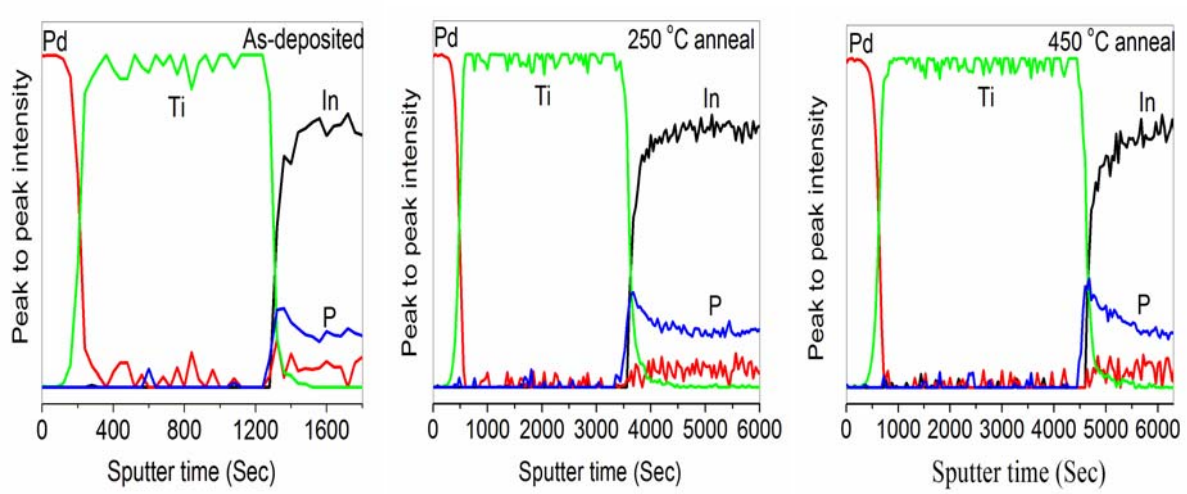

Fig. 4. Auger depth profile of the Pd/Ti Schottky contact to n-InP: (a) as-deposited, (b) annealed at 250 °C and (c) annealed at 450 °C

X-ray diffraction (XRD) is used to identify the interfacial products that are formed before and after annealing at 450 °C. Fig. 5 shows the XRD plots of the Pd/Ti/n-InP Schottky diodes. For the as-deposited sample, Fig. 5(a), in addition to the characteristic peaks of InP (111) (222), Ti (100) and Pd (220) there are other peaks observed, which are identified as Ti_3In_4 (220) and $P_{3.20}Pd_{12}$ (313). Fig. 5(b) shows the XRD plot of the contact annealed at 250 °C. There are additional peaks observed which indicate the formation of new interfacial phases at the interface as expected from the AES result (Fig. 4(b)), compared to the as-deposited contact. These phases are identified as Ti_3In_4 (310) and Ti_3In_4 (411). When the contact is annealed at 450 °C, figure 5(c), there is an extra peak, which is identified as TiP_2 (100) in addition to the peak observed in the 250 °C annealed contact. The peak corresponding to Ti_3In_4 (411) had disappeared in the 450 °C annealed contact which is observed in the 250 °C annealed contact.

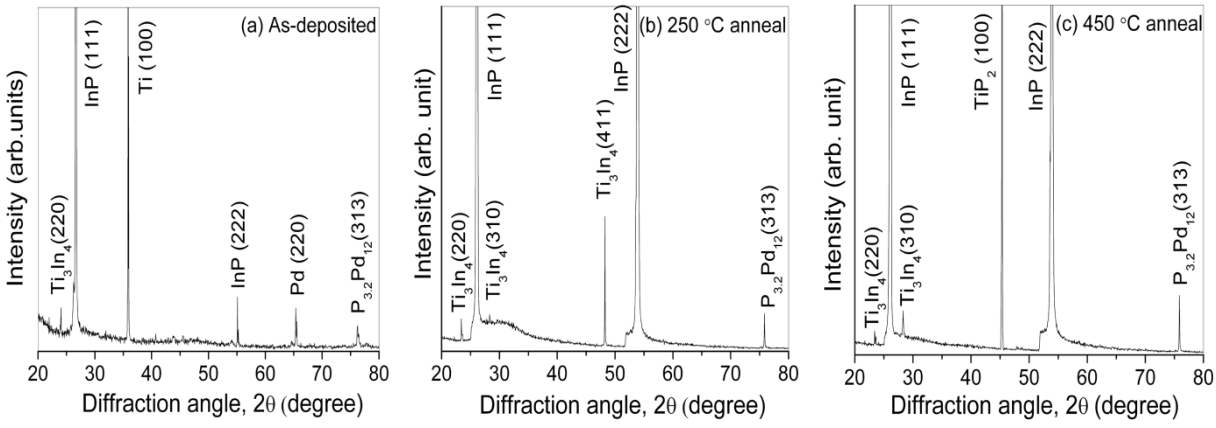

Fig. 5. XRD plots of the Pd/Ti/n-InP Schottky diode: (a) as-deposited, (b) annealed at 250 °C and (c) annealed at 450 °C.

The atomic force microscopy (AFM) is performed to characterize the surface morphology of the Pd/Ti Schottky contacts before and after annealing temperature. AFM images of the Pd/Ti Schottky contact of the as-deposited, annealed at 250 °C and 450 °C are shown in Fig. 6. The scanned area of the sample is 1×1 μm^2. It is observed that the surface morphology of the as-deposited contact is considerably smooth with a root-mean-square (RMS) roughness of 12.14 nm as shown in figure 6(a). When the contact is annealed at 250 °C, Fig. 6(b), the surface

morphology of the Pd/Ti Schottky contact becomes smother with an RMS roughness of 11.25 nm compared to the as-deposited contact. Further annealing at 450 °C, the surface morphology of the Pd/Ti contact layer becomes slightly rough with a root-mean-square (RMS) of 12.09 nm as shown in figure 6(c) as compared with that of 250 °C annealed contact. These results indicate that the overall surface morphology of Pd/Ti Schottky structure remains reasonably smooth during annealing temperatures.

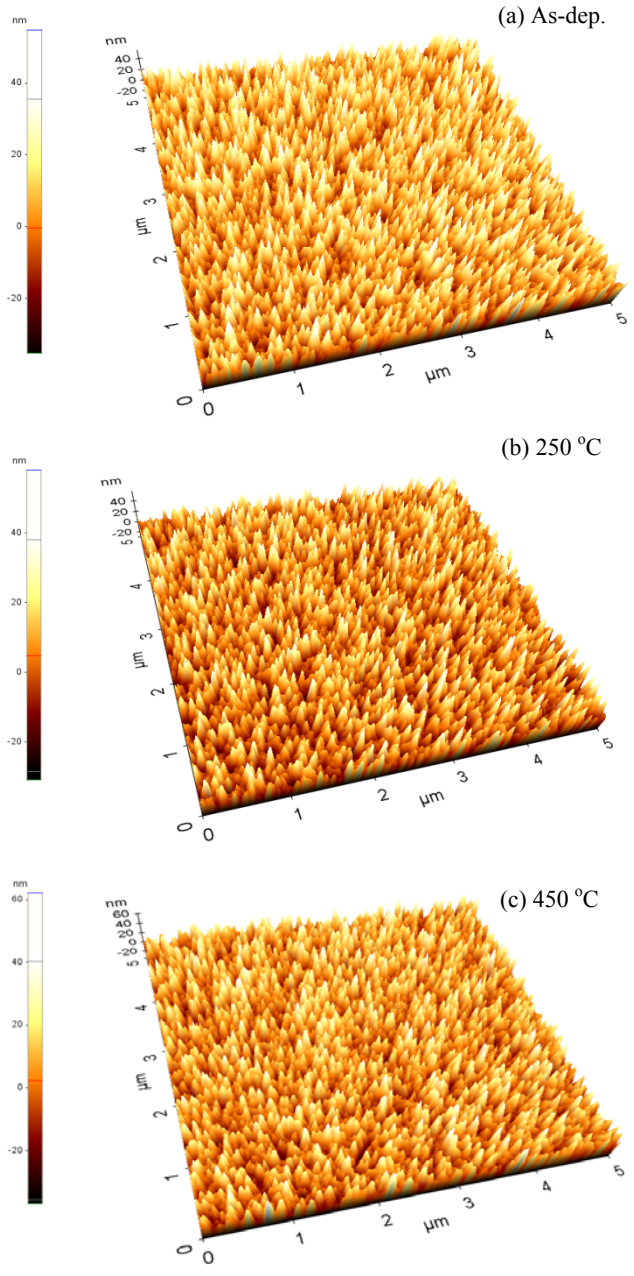

Fig. 6. AFM micrographs of the Pd/Ti Schottky contacts to n-InP: (a) as-deposited, (b) annealed at 250 °C and (c) annealed at 450 °C

Table 1. The Leakage current, Schottky barrier heights (ϕ_b) and ideality factor (n) of Pd/Ti Schottky structure on n-InP as a function of annealing temperature.

Sample (°C)	Leakage current at -1V	SBH (eV)		SBH (eV)	
		ϕ_b	n	Norde	C-V
As-dep	1.87×10^{-5}	0.58	1.46	0.64	0.79
150	1.66×10^{-5}	0.59	1.37	0.61	0.80
250	4.83×10^{-7}	0.67	1.18	0.70	0.87
350	3.85×10^{-6}	0.60	1.30	0.63	0.82
450	2.69×10^{-5}	0.54	1.64	0.59	0.73

It is well known that the chemical reactions between the metal and the semiconductor interfaces can play an important role in determining the electrical properties of devices. The degree of intermixing of In and P with the contact metal and the formation of surface states at the interface are influenced by the chemical reactivity of the metal with InP. The electrical measurements showed that the barrier height is increased for the contact annealed at 250°C compared to the as-deposited one. The improved Schottky barrier height of the Pd/Ti contact upon annealing at 250 °C, could be ascribed to the interfacial reaction occurring between metal layers and InP. According to the results of AES and XRD, the out-diffusion of the indium (In) from the InP into Pd/Ti layers and it participate in the formation of indium phases occurs at the interface. The formation of $PdIn_3$ (211), Ti_3In_4 (310) and Ti_3In_4 (411) (as shown by XRD results in Fig. 5(b)), results leads to the accumulation of indium vacancies at the InP surface region. This induces an increase in Schottky barrier height of the Pd/Ti contact which is extracted from I-V characteristics for the annealed contact at 250 °C. Another possibility is that a reduction of nonstoichiometric defects in the metallurgical interface [29] may also be the reason for the increase of Schottky barrier height. The decrease in barrier height after annealing at 450 °C may be due to the phase segregation of indium at the interface allowing relatively easy reactions between metal layers and InP which results in the formation of metal-anion complexes at higher temperatures [30]. The out-diffusion of phosphorous and its reaction with titanium resulting in the formation of interfacial compound TiP_2 (100) a metal-anion complex may be the reason for decrease in the barrier height of Pd/Ti Schottky contact after annealing at 450 °C. This finding is consistent with the results previously reported by Andersson [31] and Ivey et al [32]. They noted that the possible explanation for the disappearance of P from the near-surface region after heat treatment of the sample at high temperatures is due to the loss of volatile P to the atmosphere. The variation of SBHs of Pd/Ti Schottky contact may be due to the observed structural changes in the Pd/Ti contacts on the surface.

4. Conclusions

Based on the I-V, C-V, AES, XRD and AFM results presented here, several conclusions can be drawn as follows. The Schottky barrier height of the as-deposited Pd/Ti contact is found to be 0.58 eV and 0.79 eV (C-V). However, it is observed that the Schottky barrier height increases to 0.67 eV (I-V) and 0.87 eV (C-V) when the contact is annealed at 250 ^{o}C for 1 min in nitrogen ambient. Further, when the sample is annealed at 450 ^{o}C, the barrier height slightly decreases to 0.54 eV (I-V) and 0.73 eV (C-V) respectively. It is noted that the I-V characteristics of the Pd/Ti/n-InP Schottky diode show good rectification after annealing at 250 ^{o}C. Hence, the optimum temperature for the Pd/Ti Schottky contact is 250 ^{o}C. On the basis of the above observations, it is clearly stated that the Schottky barrier parameters of the Pd/Ti Schottky structure slightly change in the leakage current, SBH and ideality factor upon annealing at 350 ^{o}C and 450 ^{o}C. The change in SBH and ideality factor during annealing temperatures may be attributed to the interfacial reactions between the Pd/Ti and InP layers. The AES and XRD results showed that indium interfacial phases are formed at the interface could be the reason for the increase of barrier height for 250 ^{o}C annealed contact. The formation of phosphate interfacial phases at the interface, after annealing at 450 ^{o}C could be the reason for decrease of barrier height for Pd/Ti Schottky contact, as evidenced from the AES and XRD results. The AFM results show that the overall surface morphology of Pd/Ti Schottky contacts on n-InP is reasonably smooth. These results indicate that the Pd/Ti Schottky metallization scheme is a good choice for the fabrication of InP-based electronic device applications.

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*Corresponding author: reddy_vrg@rediffmail.com