JOURNAL OF OPTOELECTRONICS AND ADVANCED MATERIALS Vol. 9, No. 12, December 2007, p. 3795 - 3802

Electrical characteristics of nano-PbS/SiO_2/Si heterostructures obtained by chemical bath method

A. GOLDENBLUM*, V. STANCU, M. BUDA, G. IORDACHE, T. BOTILA, C. NEGRILA
National Institute of Materials Physics, Atomistilor Str. 111, Bucharest-Magurele, Romania

The PbS/SiO_2/Si structures show a clockwise hysteresis of capacitance-voltage (C-V) characteristics. The loop width increases with temperature and sweep time. The conductance-voltage (G-V) characteristics also present a hysteresis effect with two bumps. Both characteristics show a strong shift with frequency . We show that these effects are determined by the positive mobile ions injected in the oxide region during the chemical bath deposition of PbS and by the high concentration of Si/SiO_2 interface states. The corresponding C-V and G-V characteristics are simulated and the main peculiarities of the experimental results are well reproduced by the modeled curves.

(Received November 30, 2007; accepted December 4, 2007)

Keywods: Semiconductor devices, Electrical characteristics, Hysteresis

1. Introduction

PbS is a narrow gap semiconductor with many applications in optoelectronic devices [1]. Recently, lead sulphide layers with nano-range particles were obtained by chemical bath deposition (CBD) [2],[3],[4] and sol-gel methods [5]. They show a strong quantum size effect, allowing for the extension of the applications range from the infrared to the visible region of spectra. By incorporating the PbS layers into heterostructures it is possible to design a new variety of optoelectronic devices. Thus, photovoltaic cells with PbS/Si heterojunctions were realized [6],[7]. PbS was also deposited on other types of semiconductors or even on ferroelectric ceramics [8]. More complex devices using both microcrystalline and nanocrystalline PbS layers were also reported. Thus, metal-semiconductor-insulator-semiconductor-metal (MSISM) structures were manufactured using silicon nitride (Si_3N_4) [9] or silicon dioxide (SiO_2) [10] as an insulator and microcrystalline PbS and crystalline Silicon as a semiconductor. Using a "field effect geometry" it was shown that it is possible to tune the photoconductive signal in PbS by the applied gate voltage [10]. More recently a similar effect was reported for nanocrystalline PbS. In this case the ratio between the infrared and visible signals could be tuned in a very large range by varying the gate voltage [3]. Some other unusual phenomena were observed in these structures. They show large hysteresis loops in both capacitance-voltage (C-V) and the conductance-voltage (G-V) characteristics as well as a strong shift with frequency. In this paper we analyze in detail these phenomena.

Large hysteresis effects in the C-V characteristics were reported in the early stage of MOS devices development. They are determined mostly by the sodium positive mobile ions as it was shown first by Snow, Grove, Deal and Sah [11].

Hysteresis phenomena were recently reported in MIS structures involving high-k dielectrics and also in silicon on insulator nanocrystal memories. For ZrO_2 based structures, swept from accumulation to inversion and backwards, it was observed a shift of the capacitance-voltage characteristics, of 45 mV [12]. In the case of yttrium oxide (Y_2O_3) a maximum shift of about 200 mV for a sweep rate of 0.1V/s was found [13]. A significant wider hysterezis of the order of a few Volts was observed in metal-insulator-semiconductor memory structures with nanocrystals (Si, Ge, HfO_2) in oxide matrices [14],[15]. The exact discharge and retention mechanisms are still under debate but it looks like they are related to the interface states. We have studied structures, with nano-PbS on SiO_2 and we found a shift of about 3V for a sweep rate of 0.01 V/s. Other unusual aspects of the C-V and G-V characteristics were also observed in these structures. A simulation of the observed effects was developed using simple approximations for the structures under test and for the trap distribution at the interfaces.

2. Sample preparation and device characterization

The PbS films were deposited on Si/SiO_2 substrates by chemical bath deposition (CBD). The Pb^{2+} ions are precipitated from a 0.06M $PbNO_3$ solution by the S^{2-} ions from a 0,24M SC $(NH_2)_2$ solution. The pH of the depositon bath is adjusted using NaOH. The nanocrystalline thin film was obtained from the reducing bath without doping elements after a short reaction time of about 17 minutes at 24 ^oC. The substrates were p-Si (100) wafers with resistivity of about 30 Ωcm and a 200 nm thick SiO_2 layer.

The electrical contacts were made of Al on Si and Au on PbS. The Au contact dot area was 1.5 mm^2. In the following we call the Au/PbS/SiO_2/Si/Al structure as

$PbS/SiO_2/Si$ and the simple MOS device $Au/SiO_2/Si/Al$ as $Au/SiO_2/Si$ structure.

The chemical deposition was followed by a thermal treatment of 400 h in air at 80 ^oC for all samples. It was found that this thermal treatment drastically improve the photoconductive sensitivity of the PbS layers.

The C-V and G-V small-signal characteristics were measured using an Agilent bridge and the I-V curves under dark conditions were recorded using a Keithley dc source and an electrometer

From the photoelectric measurements we estimated the average grain size in the nanocrystallite films of about 3.8 nm. The sheet resistance of the nanocrystalline layers is more than one order of magnitude larger than for the microcrystalline layers. In p-PbS microcrystalline films the hole concentration is relatively large (10^{17} cm^{-3}) [5]. In nanocrystalline films a higher sheet resistance could be determined by a reduced carrier density and/or a reduced mobility, due to an increased number of intergrain barriers.

3. Experimental results

The C-V and G-V characteristics of nanocrystalline-$PbS/SiO_2/Si$ structures show hysteresis loops at room temperature as presented in Fig.1 for a sweep voltage range of ±5V. A clockwise hysteresis in the C-V characteristics can be observed for all investigated frequency values. An other unusual aspect is the large, nearly-parallel, shift of the C-V curves, with frequency.

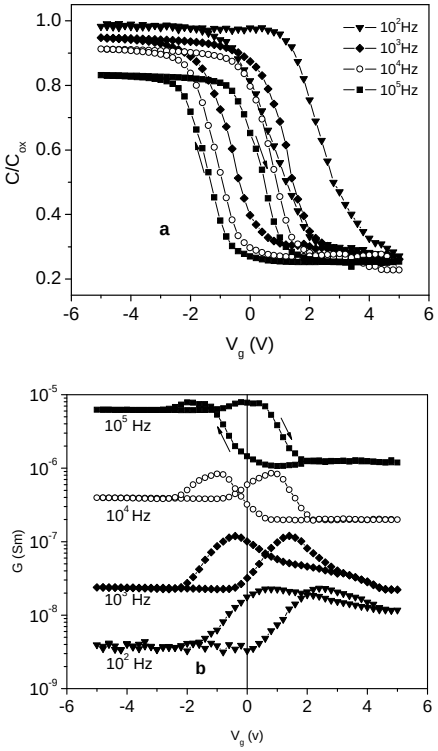

Fig. 1. Capacitance-Voltage (a) and Conductance – Voltage (b) characteristics of a $PbS/SiO_2/Si$ structure. Maximum sweep voltage ± 5 V, total sweep time 906 s. The arrows illustrate a hysteresis loop.

The G-V characteristics also show hysteresis phenomena with two "bumps" and a very large shift of the curves with frequency.

The width of the hysteresis loops for a certain maximum sweep voltage increases with the sweep time and the temperature but is not frequency dependent.

Each branch of the high frequency C-V characteristics, as in Fig. 1a, looks like an usual C-V curve of a MOS structure. Therefore the clockwise hysteresis can be a consequence of a flat voltage shift due to the positive mobile charge in the oxide region. We prove this by removing the PbS layer in HCl solution and depositing a Au contact on the free oxide surface to obtain a MOS structure. Fig. 2 shows again the presence of the hysteresis even if the PbS is absent. Therefore the effect is not related to the presence of the PbS layer but is determined by the positive charge present in the *oxide region* due to a diffusion process during the chemical bath deposition and the thermal treatment.

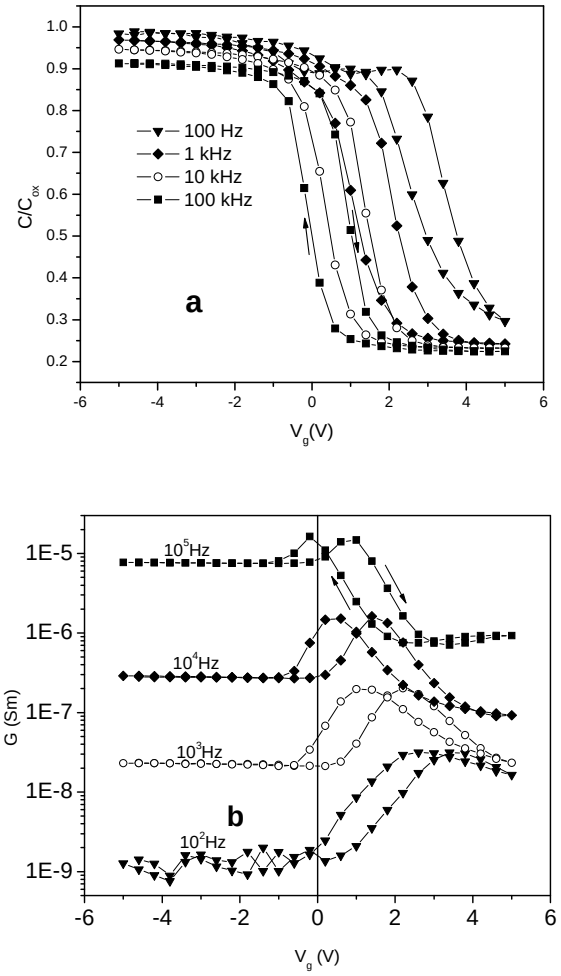

Fig. 2. Capacitance-Voltage (a) and Conductance – Voltage (b) characteristics of a $Au/SiO_2/Si$ structure. Maximum sweep voltage: ±5 V, total sweep time: 152 s.

4. Analysis

As the interpretation of the experimental data corresponding to a simple MOS structure is less complicated than for a complex heterostructure involving PbS, we begin our analysis with the MOS structure and we will extend it afterwards.

It is well known that usually the hysteresis effects in Si/SiO_2 based MOS devices are related to the presence of mobile positive Na ions in the oxide region. It is most probable that this also happens in our structures due to the presence of the sodium ions in the growth bath solution.

The induced charge on the Silicon interface determined by the positive Na ions is given by [15]:

$$Q_i = -\frac{1}{d_{ox}} \int_0^{d_{ox}} x\rho(x)dx \qquad (1)$$

where ρ(x) is the charge distribution, x being the distance measured from the gate.

A positive gate bias, causes the mobile charge to move away from the gate electrode and to accumulate at the Si/SiO_2 interface. Therefore, in this situation, the induced charge has the maximum value in eq. (1) and then we have:

$$Q_i \approx -\int_0^{d_{ox}} \rho(x)dx = -Q_{os} \qquad (2)$$

where Q_{os} is the charge accumulated in a given time at the Si/SiO_2 interface.

Applying a negative gate bias, the mobile ions return to the SiO_2/gate interface and Q_i becomes negligible. A sweep cycle thus results in a flat voltage shift given by:

$$\Delta V = -\frac{Q_{os}}{C_{ox}} \qquad (3)$$

that determine the hysteresis behavior of the C-V characteristics.

The quantitative analysis was made by Snow et al.[11] for the simple case of a constant positive bias applied for a given time, when the ions are transported from the metal-oxide to the oxide-semiconductor interface. They assume a high uniform initial concentration of ions within a small region of width x_1 near the metal-oxide interface and a zero concentration through the rest of the oxide. Applying the gate voltage, there will be no electric field in the main part of the oxide, but a negative one near the metal-insulator interface due to the image charge induced in the metal. When a positive bias is applied, the field is divided between this small region and the rest of the oxide. In the above mentioned small region the applied positive field is summing up with the negative image charge field and then a relative low value results for the total field. Therefore the transport process in this part of the structure is determined by the diffusion of the mobile ions due to the concentration gradient and not by a field controlled drift. In the rest of the oxide the high field ensures a quick transport of the ions toward the oxide-silicon interface where they accumulate. Consequently, the entire transport process is controlled by the ion diffusion process from the small region of the accumulated charge near the metal-oxide interface. Thus, the rate of ion accumulation near the oxide-silicon interface equals the rate of their depletion from the opposite interface. The latter is given by the flux of the diffusing ions at the edge of the small region x_1 and therefore the accumulated charge at the oxide-silicon interface in time will be:

$$Q_{os} = -q\int_0^t D\frac{\partial N}{\partial x}(x_1 t')dt' \qquad (4)$$

Solving the diffusion equation in the region of the metal-oxide interface Snow et al. have found two simple asymptotic solution for Q_{os}, i.e.:

$$Q_{os} \cong \frac{4Q_0}{\pi^{\frac{3}{2}}}\left(\frac{t}{\tau_h}\right)^{\frac{1}{2}} \quad \text{for } t<<\tau_h \qquad (5)$$

and

$$Q_{os} \cong Q_0\left(1-\frac{8}{\pi^2}e^{-\frac{t}{\tau_h}}\right) \quad \text{for } t>>\tau_h. \qquad (6)$$

where Q_0 is the total mobile positive charge assumed to be constant during the whole ion drifting process and

$$\tau_h = \frac{4x_1^2}{\pi^2 D} \qquad (7)$$

The model presented above is built up for a constant field applied for a given time t. However the field does not appear explicitly in expressions (5) or (6). This happens because the entire process is controlled by the ion diffusion from the small band of ions accumulated at the metal-oxide interface. Therefore the model can be applied even if the field varies in time during a sweep process and the important parameter is only the time of ion collection, i.e. in our case the time of positive biasing.

Then we have for the flat band shift after the time t_p of applying the positive bias:

$$\Delta V = -\frac{4Q_0}{\pi^{\frac{3}{2}}C_{ox}}\left(\frac{t_p}{\tau_h}\right)^{\frac{1}{2}} \quad \text{for } t_p << \tau_h \qquad (8)$$

or

$$\Delta V = -\frac{Q_0}{C_{ox}}\left(1-\frac{8}{\pi^2}e^{-\frac{t_p}{\tau_h}}\right) \quad \text{for } t_p>>\tau_h. \qquad (9)$$

These two solutions match in the intermediate ratio of t_p/τ_h so that, for example, the second equation could be used until 0.25 of this ratio as presented in Fig. 12 of the reference [11].

Other peculiarities of the C-V characteristic, especially their shift with frequency, are connected with the *silicon-insulator interface states*. It is usually considered that the interface trap capacitance is determined by a single time constant . However the deeper levels emit carriers with a lower probability than the shallow levels when the Fermi level moves further away from the valence band edge [16]. In the following we will take into account the surface potential dependence of time constant which shapes both the C-V and G-V characteristics.

A small harmonic gate voltage variation is followed by a small variation of the silicon surface potential δu_s. Consequently, the small variations of the semiconductor space charge and of the Si/SiO2 interface charge are given by:

$$\delta Q_s = C_s \delta u_s \tag{10}$$

$$\delta Q_{it} = q \int_{E_v}^{E_c} D_{it}(E_t)\delta f_{it} dE_t = C_{it}\, \delta u_s \tag{11}$$

where D_{it} is the density of Si/SiO_2 interface states, δf_{it} is the trap level occupation probability deviation from its equilibrium value. C_s is the semiconductor capacitance and C_{it} the equivalent interface state capacitance.

Supposing that each trap exchanges carriers only with the valence band the corresponding rate equation is:

$$\frac{df_{it}}{dt} = c_{ps} p_s - c_{ps} f_{it}\left(p_s + \frac{e_{ps}}{c_{ps}} N_v\right) \tag{12}$$

where: c_{ps} is the trap capture coefficient; e_{ps} the emission coefficient, N_v is the density of states in the valence band and p_s is the density of carriers in this band at the interface. The ratio of the two coefficients is:

$$\frac{e_{ps}}{c_{ps}} = e^{-(E_t - E_v)/kT} \tag{13}$$

In depletion $p_s = N_v e^{-\frac{E_F - E_v}{kT}}$ (14)

The rate equation becomes:

$$\frac{df_{it}}{dt} = c_{ps} p_s - \frac{f_{it}}{\tau} \tag{15}$$

where the trap relaxation time is given by:

$$\tau = \frac{\tau_o}{e^{-(E_t - E_v)/kT} + e^{-(E_F - E_v)/kT}} \tag{16}$$

$$\tau_o = \frac{1}{c_{ps} N_v} \tag{17}$$

Taking into account that the Fermi level position is connected to the surface potential by:

$$E_F - E_v = q u_s + \eta \tag{18}$$

the interface capacitance can be obtained from Eq. (11)

$$C_{it} = \frac{\delta Q_{it}}{\delta u_s} = q \int_{E_v}^{E_c} D_{it}(E_t) \frac{\delta f_{it}}{\delta u_s} dE_t \,. \tag{19}$$

For a small a.c. signal of frequency ω the hole density at the surface varies like:

$$p_s = p_{s0} e^{j\omega t} \tag{20}$$

and from eq. (15) we obtain:

$$\delta f_{it} = \frac{\delta f_{it0}}{1 + j\omega\tau} \tag{21}$$

Then the interface capacitance will be:

$$C_{it} = \frac{q^2}{kT} \int_{E_v}^{E_c} D_{it}(E_t) \frac{e^{(E_t - E_F)/kT}}{(1 + e^{(E_t - E_F)/kT})^2} \frac{1}{1 + \omega^2 \tau^2} dE_t \tag{22}$$

and the conductance:

$$G_{it} = \frac{q^2}{kT} \int_{E_v}^{E_c} D_{it}(E_t) \frac{e^{(E_t - E_F)/kT}}{(1 + e^{(E_t - E_F)/kT})^2} \frac{\omega^2 \tau}{1 + \omega^2 \tau^2)} dE_t \tag{23}$$

We observe that the emission rate depends strongly on the difference between the trap energy and that corresponding to the valence band (eq.13). The value of τ is higher for deeper levels than for shallow interface levels as we can see in eq. (16). Therefore only the interface traps situated not far from the valence band edge contribute significantly to the interface capacitance. Assuming a uniform distribution of traps beginning from the edge of the valence band we see in Fig. 3 that the interface capacitance at low voltage has a constant value first and then it drops drastically, for a given voltage that depends on frequency.

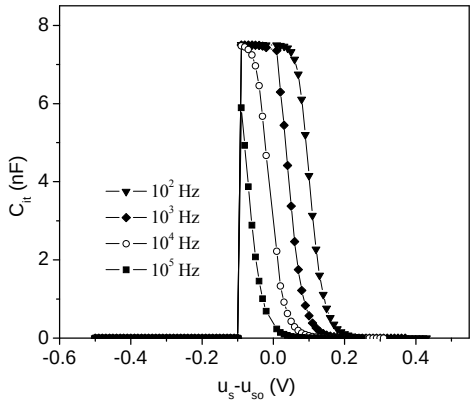

Fig. 3. The dependence of the interface capacitance on surface potential for different frequency values. u_{so} is the surface potential value at the zero bias. Main computation parameters: $\tau_0 = 10^{-5}$ s, $D_{it}=3.1\times10^{12}cm^2eV^{-1}$, area= 1.5 mm^2.

We will further use the well known equivalent circuits describing the a.c response of a MOS structure for all three distinct functional regimes: accumulation, depletion and inversion.

In depletion the usual equivalent circuit has the oxide capacitance (C_{ox}) in series with the group of semiconductor capacitance (C_s) in parallel with the interface states capacitance (C_{it}) and conductance (G_{it}) [17]). The total admittance is**:**

$$Y = G + j\omega C$$

with:

$$G = \frac{\omega^2 G_{it} C_{ox}^2}{G_{it}^{\ 2} + \omega^2 (C_{ox} + C_s + C_{it})^2} \tag{24}$$

$$C = \frac{C_{ox} G_{it}^2 + \omega^2 (C_{ox} + C_s + C_{it}) C_1 (C_s + C_{it})}{G_{it}^2 + \omega^2 (C_{ox} + C_s + C_{it})^2} \tag{25}$$

In weak accumulation eq. (15) is not valid anymore. The single level approximation is now adequate, i.e.:

$$C_{it} \approx q^2 D_{it}$$
$$G_{it} \approx \omega^2 \tau_0 C_{it} \tag{26}$$

In accumulation we must take into account the effect of the structure series resistance. In this case the equivalent circuit [17]) has the oxide capacitance in series with the above mentioned group of C_s, Cit, G_{it} and with the series resistance R. Then the total admittance is:

$$Y = \frac{\omega^4 C_{ox}^2 C_2^2 R + j\omega\left[\omega^2 C_{ox1} C_2 (C_{ox} + C_2)\right]}{\omega^4 C_{ox}^2 C_2^2 R^2 + \omega^2 (C_{ox} + C_2)^2} \tag{27}$$

where:

$$C_2 = C_s + C_{it} \tag{28}$$

Then the corresponding capacitance and the conductance are respectively:

$$C = \frac{C'}{1 + \omega^2 \tau_{ef}^2} \tag{29}$$

$$G = \frac{\omega^2 \tau_{ef} C'}{1 + \omega^2 \tau_{ef}^{\ 2}} \tag{30}$$

with:

$$C' = \frac{C_{ox} C_2}{C_{ox} + C_2} \tag{31}$$

and $\tau_{ef} = R \dfrac{C_{ox} C_2}{C_{ox} + C_2}$ (32)

In strong accumulation regime C_{it} drops to zero and $C_2 = C_s$.

For positive bias that get the Silicon region in weak inversion the space charge capacitance value become $C_s = C_{s\min}$ in the investigated frequency range. At the same time C_{it} becomes very small and at high voltage, G_{it} also drops drastically for the same reason presented above (see Fig. 3) . However, we must take now into account the presence of the minority carriers. In this case, the generation-recombination process can be described successfully by a single time-constant τ_r [18] that can be represented in an equivalent circuit by a group of a capacitance C_r in series with a resistance R_r. Therefore the conductance value becomes:

$$G_2 = \frac{\omega^2 \tau_r C_r}{1 + \omega^2 \tau_r^2} + G_s \tag{33}$$

where $\tau_r = R_r C_r$ is the generation-recombination life-time and G_s is the conductance associated with the carrier flow toward the interface [18]. To have a strong frequency dependence for high frequency as we have learned from the experiment, we must have: $\omega\tau_r << 1$ and therefore:

$$G_2 \approx \omega^2 \tau_r C_r + G_s .$$

Thus, the total conductance will be:

$$G \approx \frac{\omega^2 G_2 C_{ox}^2}{G_2^{\ 2} + \omega^2 (C_{ox} + C_s)^2} \tag{34}$$

The applied voltage V_G is divided between the oxide and the space charge region:

$$V_G - \Phi_{ms} = u_s + u_{ox} = u_s + \frac{Q_s + Q_{it} + Q_i}{C_{ox}} \tag{35}$$

where Q_s (the space charge) and u_s can be evaluated from the Poisson's equation [18]. Φ_{ms} is the metal-semiconductor work function difference.

For a simulation of the phenomena presented above we will use some parameters that are extracted directly from the experimental data as the hole concentration of $5x10^{14}$ cm^{-3} from the resistivity of the Silicon material. The corresponding Fermi level in the neutral region and the value of Φ_{ms} corresponding to this hole concentration are η=0.247 V and 0.02 V respectively. A small flat band shift of high frequency capacitance to the right of about 0.15 eV was also determined. We used as a hysterezis shift the value in Fig. 1 to allow for a direct comparison between the computed and the experimental curves.

Fig. 4 shows the simulation of the investigated phenomena for both C-V and the G-V characteristics for a structure with uniform distribution of traps at the Si/SiO_2 interface using equations (22) - (35). Only one or two free parameters for each region (accumulation, depletion, inversion) were used for computations: $\tau_0= 10^{-5}$ s, $D_{it}=3.1 \times 10^{12}$ $cm^{-1}eV^{-1}$, R= 1×10^3 Ω, $C_r\tau_r=2 \times 10^{-16}$ Fs ,$G_s=2 \times 10^{-9}$ Sm.

One can observe, by comparison with Fig. 1, that the simple model of uniform distributed interface states describes well qualitatively *the nearly-parallel frequency shift of the C-V and G-V curves*.

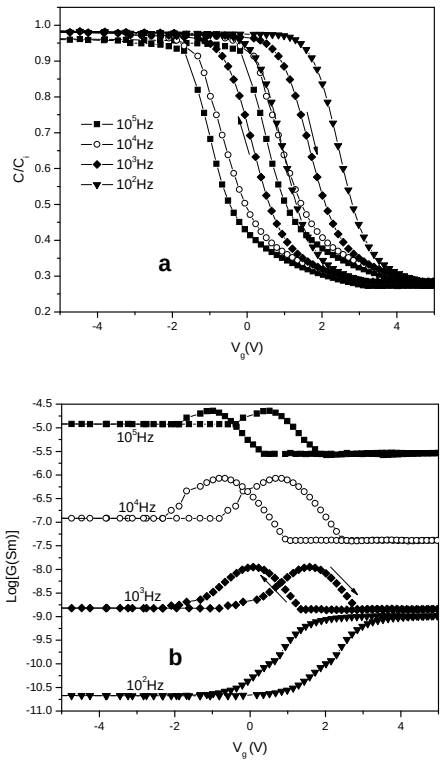

Fig. 4. Computed C-V (a) and G-V (b) characteristics.

The model even describes some fine details in the shift of the C-V curves with frequency. Thus, the 10^4 Hz curve is much less shifted relative to the 10^5 Hz curve as for example the 10^2 Hz curve relative to the 10^3 Hz. The nearly-parallel shift with frequency is determined by the fact that even if the semiconductor capacity C_s decreases to its minimum value, the capacitance $C_2 \approx C_{it}$ can have a much higher value than C_{ox} and therefore the total capacitance is further equal with C_{ox} until the interface capacitance drops and therefore the fall is shifted with frequency due to the behavior of C_{it} presented in Fig. 3.

A frequency shift of the C-V curves determined by the contribution of ionized interface centers is well known [16]. However, this shift is not parallel. The nearly-parallel shift is determined by the abrupt parallel drop of the interface capacitance for different frequency values as shown in Fig. 3. This drop occurs within a small voltage range and the corresponding flat-voltage shift does not change the shape of the curve.

The presence of the bumps in the G-V characteristics is determined by the increase of the density of states near the $Si-SiO_2$ interface and by the fall of their corresponding G_{it} conductance values as described by (18), similar to C_{it} as shown in Fig. 3. The bumps shift to the right, as the frequency decreases, has the same origin as the frequency shift of the C-V curves.

There is no significant difference in the behavior of C-V and the G-V characteristics between the $PbS/SiO_2/Si$ and $Au/SiO_2/Si$ structures as we can observe comparing Figs. 1 and 2. This shows that the PbS series capacitance is large enough to have no major influence on the characteristics. Indeed, the relative dielectric constant of PbS is very high (170) and the PbS layer thickness is less than 100 nm. However, we see in Fig. 1a that the accumulation branch of the 10^5 Hz capacitance has a much lower value than that of the structures without PbS layers. This indicates that the PbS layer creates a capacitance with high losses due to the considerable conductance of the PbS nano-layer and the corresponding "series resistance" shifts down the low frequency accumulation branch [17], [19].

The predictions of the Snow's model of hysteresis are compared to the experimental data concerning the time and temperature dependence of the loop width. We evaluate them by measuring the hysteresis parallel shift of the experimental curve at the middle of the C-V curve.

The experimental data, for the same maximum sweep voltage (5V) are shown together with the curve calculated using eq. 9 in Fig. 5. It shows a good fit for a time constant of 257 s. We mentioned above that this formula is valid even for sweep time comparable with τ_h.

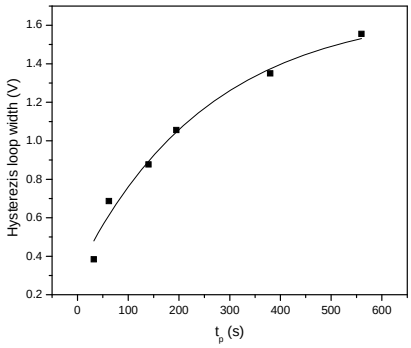

Fig. 5. Hysteresis loop width dependence on the positive bias time. The solid line is the result of fit with formula 9.

As far as the temperature dependence of the flat band shift is considered, this is included in the time constant τ_h (Eq. 7) which is proportional to the reciprocal of the diffusion coefficient D that has the form of:

$$D = D_0 e^{-\frac{\Delta E}{kT}} \tag{31}$$

with ΔE the activation energy of the diffusion process.

Therefore the time constant τ_h depends strongly on temperature. It is expected to have larger values for temperature lower than room temperature such as $t_p << \tau_h$. In this case the equation 9 is valid and we have:

$$\Delta V = -\frac{2Q_0}{\pi^{\frac{1}{2}} x_1} (t_p D_0)^{\frac{1}{2}} e^{-\frac{\Delta E}{2kT}} \tag{32}$$

As we mentioned above this formula can be extended even for time values comparable to the time constant.

An Arrhenius plot of the temperature dependence of the hysteresis shift for the same sweep time and the same maximum sweep voltage gives a straight line (Fig. 6) in accordance with formula (32). The extracted value of the activation energy ΔE is 0.43 eV.

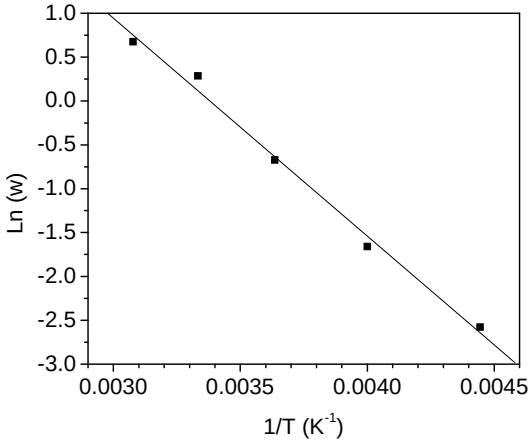

Fig. 6. Temperature dependence of the loop width in an Arrhenius plot. Maximum sweep voltage: ±5 V, positive biasing time: 415 s.

This value is significantly different from those reported by some authors (ex. 0,7 eV [20]). However it coincides with the value found by others [21] which suggest some reasons for this difference by considering that the ion diffusion behavior can be influenced by the structural and purity of the oxide. We must mention also that our measurements were made within a temperature range lower than those reported in literature.

Some disagreement between the predictions of the simple model of uniform interface states and the experimental G-V characteristics can be observed. Thus, using single values for each time constants τ_o, τ_{ef}, τ_r in the whole range of frequency, the calculated G values vary in a much extended range than we have found experimentally, as we can observe comparing the characteristics presented in Figures 1b and 4b. This fact suggests that at the Si/SiO_2 interface there are different species of states, some of them with time constant larger than others and thus responding better to the low frequency signals. In this way the product $\omega^2\tau$ becomes larger and therefore the curves are shifted up.

Although the interface states can be involved in the mechanism of hysterezis in solid-state memory devices, in our case they are not a determining factor. A large density of interface states is revealed in MOS-type devices without hysterezis in the C-V characteristics [16]. In our devices, the time constant of interface effects obtained from modeling is much smaller (10^{-5} s) than the one associated with the hysterezis (t_h of the order of 10^2 s) such that the effect of the interface states on the hysterezis is ruled out.

5. Conclusions

We evidenced large hysterezis effects in both C-V and G-V characteristics of nano-PbS/SiO_2/Si structures. We have demonstrated that the hysterezis effect is not related directly to the presence of a PbS nano-layer. The effect is determined by the presence of sodium ions in the oxide region as a consequence of the chemical bath deposition method used for the PbS layer, as solutions with sodium compounds were used.

This study allows us to prove that the Snow et al. model describes very well the hysteresis effect in a sweep regime, which is different from the initial reported method of drifting the ions in a constant field.

We also analyzed another interesting behavior of the C-V and G-V characteristics, namely their nearly-parallel large shift at low frequency. We demonstrated that this effect is determined by the Si/SiO_2 interface states that emit carriers with longer time constant as the Fermi level scans deeper into their distribution. The consequence is that the interface capacitance for a uniform state distribution in energy is about constant at the beginning of the sweep process until it drops at a certain applied voltage for a given frequency value. In fact, in real structures the distribution is not uniform. However, in most cases the density of interface states is larger near the extended band edges and then drops towards the center of the gap. On the other hand the abrupt fall mentioned above is not very sensitive to the interface state concentration as long as the value of interface capacitance is much larger than the capacitance of the semiconductor. Therefore, the frequency shift is qualitatively the same for a moderate variable high concentration as for the uniform distribution of the interface states as well.

Acknowledgements

This work was supported financially by the Romanian Ministry of Education and Research in the frame of the CNCSIS grant No. GR 124/03.05.2006 and the nucleus program No. 41N/24.01.2006. We are grateful to dr. E. Pentia for the excellent quality of samples used for this work.

References

[1] R. H. Bube, Photoelectric Properties of Semiconductors, Cambridge University Press, Cambridge 1992.
[2] Rakesh K. Joshi, Aloke Kanjilal, H. K. Sehgal, Appl. Surf. Science **221**, 43 (2004).
[3] M. Buda, V. Stancu, E. Pentia, T. Botila, Proc. 2006 International Semiconductor Conference, Sinaia-Romania, IEEE editor, 2006, IEEE Catalog Number 06TH8867.
[4] R. S. Patil, H. M. Patan, T. P. Gujar, G. T. Lokhande, J. Mater. Sci. **41**,5723 (2006).
[5] T. Saraidarov, D. Reisfeld, A. Sashchiuk, E. Lifshitz, J. of Sol-Gel Science and Technology **26**, 533 (2003) and **34**, 137 (2005).
[6] Andrew J. Steckl, Hamman Elabd, Ka-Yee Tam, Shey-Ping Shen, M. E. Motamedi, IEEE Transactions on Electron Devices **27**, 126 (1980).
[7] I. Pintilie, E. Pentia, L. Pintilie, D. Petre, C. Constantin, T. Botila, J. Appl. Phys. **78**, 1713 (1995).
[8] I. Pintilie, L. Pintilie, V. Dragoi, D. Petre, T. Botila, Appl. Phys. Lett. **71**, 1104 (1997).
[9] L. Pintilie, E. Pentia, I. Pintilie, T. Botila, Appl. Phys. Lett. **76**, 1890 (2000).
[10] L. Pintilie, E. Pentia, I. Matei, I. Pintilie, E. Ozbay, J. Appl. Pys. **91**, 5782 (2002).
[11] E. H. Snow, A. S. Grove, B. E. Deal, C. T. Sah, J. Appl. Phys. **36**, 1664 (1965).
[12] J. C. Wang, S. H. Chiao, C. L. Lee, T. F. Lei, Y. M. Lin, M. F. Wang, S. C. Chen, C. H. Yu, M. S. Liang, J. Appl. Phys. **92**, 3936 (2002).
[13] V. Ioannou-Sougleridis, G. Velianitis, A. Dimoulas, J. Appl. Phys. **93**, 3982 (2003).
[14] C. L. Heng, T. G. Finstad, Physica E **26**, 386-390 (2005).
[15] Y.-H. Lin, C.-H. Chien, C.-T. Lin, C.-Y. Chang, T.-F. Lei, IEEE Electron Letters **3**, 154 (2005).
[16] A. Goldenblum, I. Pintilie, M. Buda, A. Popa, M. Lisca, V. Teodorescu, A. Dimoulas, G. Vellianitis, J. Appl. Phys, **99**, 064105 (2006).
[17] E. H. Nicollian, J. R. Brews, MOS (Metal Oxide Semiconductor) Physics and Technology, John Wiley & Sons, New York, 1982.
[18] S. M. Sze, Physics of Semiconductor Devices, second edition, John Wiley & Sons, New York, 1981.
[19] K. S. K. Kwa, S. Chattopadhyay, H. D. Jankoic, S. H. Olsen, L. S. Driscoll, A. G. O'Neill, Semicond. Sci. Technol. **18**, 82 (2003).
[20] E. I. Goldman, A. G. Zhdan, G. V. Chucheva, J. Appl. Phys. **89**, 130 (2001).
[21] G. Greeuw, J. F. Verwey, J. Appl. Phys. **56**, 2218 (1984).

*Corresponding author: galfred@infim.ro