JOURNAL OF OPTOELECTRONICS AND ADVANCED MATERIALS Vol. 9, No. 2, February 2007, p. 402 - 405

Electrical characterization of MOS structures with 10 nm SiO_2, thermally grown on plasma hydrogenated (100)-pSi

E. HALOVA[a*], S. ALEXANDROVA
[a]*Technical University, 8 Kl. Ohridski Blvd., Sofia 1797, Bulgaria*
Institute of Solid State Physics, Bulgarian Academy of Sciences, 72 Tzarigradsko Chaussee Blvd., 1784 Sofia, Bulgaria.

In this paper, we have focused on the electrical properties of the SiO_2/p-type Si(100) interface, where the thin silicon oxide layer was thermally grown on rf plasma-hydrogenated silicon structures. The results concerning the interface properties of the MOS structures are reported from a detailed study of the *C-V* and *G-V* characteristics at varying frequencies between 500 Hz and 300 kHz. From frequency characterization, information is gained on the charged defects at the Si/SiO_2 interface. The frequency dispersion properties reveal the presence of either interface traps or a laterally inhomogeneous distribution of defect centres within the oxide near the interface Si/SiO_2. From frequency characterization information is gained on the concentration of charged defects, and their location in the Si/SiO_2 interface region. A procedure is suggested to overcome the problem with the usually observed increase in the leakage through the oxide on p-Si, which hinders the accurate determination of the interface trap densities even in thicker oxides. We have studied and compared the effect of a rf hydrogen plasma on the silicon structures. The amount and nature of the defects depend on the substrate temperature during plasma exposure, and on the Si orientation.

(Received Novemebr 1, 2006; accepted December 21, 2006)

Keywords: Thermal SiO_2, Plasma hydrogenation, Interface charges

1. Introduction

For over four decades, Si-based technology has almost exclusively relied on the extremely convenient physical properties of the interface between crystalline silicon and its thermal oxide. In the present generation, as oxides grow thinner and thinner, the transition region at the interface between the Si substrate and the gate oxide constitutes a significant fraction of the device, calling for an atomic scale understanding of the fundamental processes occurring at the interface [1-3]. Such processes include the oxidation mechanism, the role of hydrogen and the defect generation process.

High temperature oxidation is a well established technological process for thin films used for instance as the gate or field oxide in CMOS devices. As the device dimensions shrink, there is a vital interest in being able to produce thin oxides of a quality meeting the industrial requirements in a low temperature process. Reducing the oxidation temperature, however, brings about a reduced oxidation rate, requiring unacceptably long oxidation times, especially for (100)Si, since this Si surface is characterized by lowest oxidation rates. One possibility to increase the oxidation rate is to hydrogenate the Si surface prior oxidation [4]. The presence of hydrogen atoms in the near-surface region can be expected to interfere with the oxidation process, similarly to OH-groups in the wet oxidation. The H-species, however, as highly mobile and highly active particles, can have a different effect on the oxidation mechanism. Moreover, it is well known that hydrogen tends to attach to dangling chemical bonds, thus having a strong impact on the defect concentrations. Saturation of dangling Si bonds with hydrogen has been a master process in the silicon industry for many years, used to increase the quality of the Si/SiO_2 interface.

Recently, we have suggested a rf (radio frequency) hydrogen plasma treatment as a Si pre-oxidation cleaning procedure, allowing higher oxidation rates at oxidation temperatures of 850 ºC and below, and better oxide and interface characteristics [5]. For thicker oxides, it is well known that the oxidation rates, as well as the defect densities, for both orientations differ substantially. The oxidation rates for both (111) and (100) in the initial fast oxidation regime, where oxides with a thickness up to 10 nm are formed, become very close together. The open question is about the oxide and interface defect concentrations, which is addressed in the present study.

The aim of this work was to measure the electrical properties of Al/SiO_2/p-Si MOS devices and compare with published data on similar materials and devices. The present study examines the effect of a rf hydrogen plasma on the interface properties of MOS structures with a thin SiO_2 grown thermally over hydrogenated silicon. The results are reported from a detailed study of the *C-V* and *G-V* characteristics at different frequencies between 1 kHz and 300 kHz. From the frequency characterization, information is gained on the charged defects at the Si/SiO_2 interface.

2. Experimental

The oxides were thermally grown in dry O_2 at a temperature of 850 ºC to a thickness of about 10 nm on (100)p-Si hydrogenated wafers. Bare *p*-type (100)-oriented Si wafers of 5-10 Ohm.cm resistivity were initially treated

by typical wet RCA pre-gate oxide cleaning [6]. The next step for some of the wafers was exposure to hydrogen plasma in a rf planar unit. The wafers were located on the lower grounded plate, either unheated or at a temperature of 300 ºC. The gas pressure was 1 Torr; the input power at 13.56 MHz was 15 W. The wafers that were given an RCA clean only, served as references. For MOS capacitors, circular aluminium front contacts were thermally evaporated through shadow masks, while the back contacts consisted of full area aluminium layers. The evaporation was performed under vacuum conditions.

All *C-V* and *G-V* measurements in this work were performed at room temperature using WAYNE KERR 6425 Precision Component Analyzer in the frequency range 500 Hz to 1 MHz and a test signal of 30 mV. The measurements were taken in descending order of frequency. In accumulation, no appreciable frequency dispersion was evident up to a frequency of 300 kHz. At frequencies from 300 kHz to 1 MHz dispersion related to the contribution of the series resistance of the substrate was observed [7]. Because of this, the oxide capacitance was calculated from the MOS capacitance of the 1 kHz *C-V* curve in strong accumulation, where the series resistance contribution was negligibly small. This value was used throughout the study for estimation of the defect concentrations. The fixed oxide charge was obtained from the difference between the experimental and theoretical flatband voltages.

The leakage through the oxide was taken into account as discussed in detail below. Thus we can better resolve the peaks in the *G-V* curves that are due to the charging of the interface traps.

3. Results and discussion

In Figs. 1 and 2, typical *C-V* characteristics at different frequencies of the MOS capacitors with oxides grown on rf plasma hydrogenated (100)Si are given. In Fig. 1 the C-V curves are displayed for the case when the silicon substrate was not heated during plasma hydrogenation, while in Fig. 2 the Si substrates was hydrogenated at a temperature of 300 °C. For comparison in Fig. 3 *C-V* characteristics of the standard RCA cleaned Si oxides are given.

In all cases, the *C-V* characteristics show frequency dispersion due to the time-dependent response of the interface states. At 300 °C, the *C-V* curves show much less frequency dispersion than the unheated Si and the RCA Si.

The specific shape of the *C-V* curves at low frequencies, especially for samples without heating of the Si substrates during plasma hydrogenation in Fig 1, is usually taken as an indication of increased trap density at a certain position in the Si bandgap. However it could also be indicative of an inhomogenious distribution of the oxide charges [7].

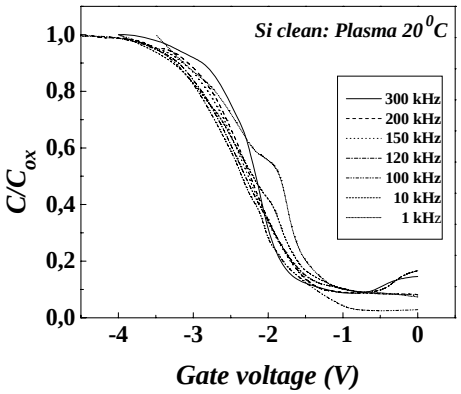

Fig. 1. Frequency dispersion of the C-V curves of MOS capacitors with SiO_2 grown on a (100)Si substrate without heating.

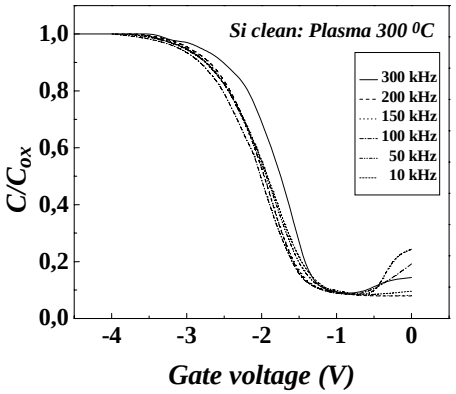

Fig. 2. Frequency dispersion of the C-V characteristics of MOS capacitors with SiO_2 grown on a (100)Si substrate at 300 ℃.

It should be mentioned that for all capacitors the C-V curve shifts do not follow the direction of the frequency change. Also, the 300 kHz curve has the highest slope. This is related to the measurement order and the presence of the so-called border traps, spatially distributed farther from the Si/SiO_2 interface into the oxide. The 300 kHz curves were the first to be measured, so that the border traps have still not captured charge carriers. As the gate voltage increased during C-V tracing, these traps were increasingly filled and caused a different C-V slope in subsequent measurements at descending frequencies.

The *G-V* characteristics of the MOS capacitors are plotted in Figs. 4 to 6. In Figs. 4 and 5, the *G-V* characteristics of the MOS capacitors are displayed for Si substrates hydrogenated without heating and with heating at 300 °C, respectively.

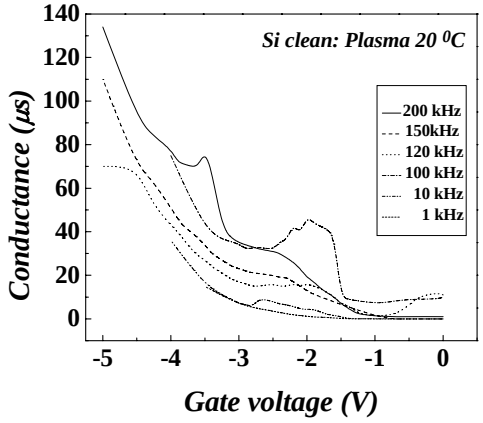

Fig. 4. Frequency dispersion of the G-V curves of MOS capacitors with SiO_2 grown on a (100)Si substrate without heating.

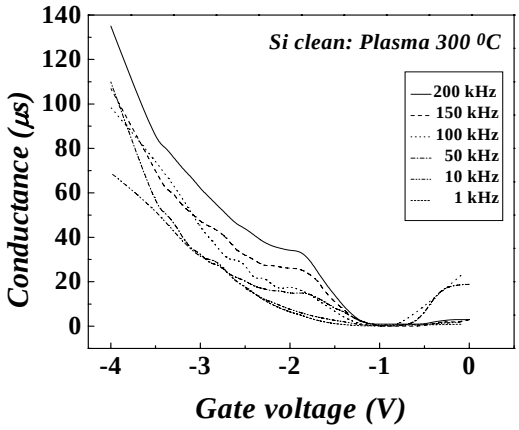

Fig. 5. Frequency dispersion of the G-V characteristics of MOS capacitors with SiO_2 grown on a (100)Si substrate at 300 ℃.

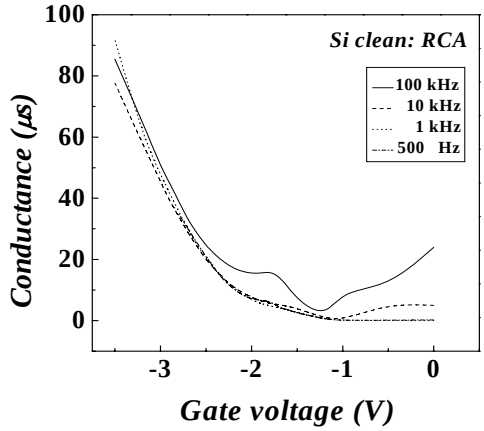

Fig. 6. Frequency dispersion of the G-V curves of MOS capacitors with SiO_2 grown on a (100)Si substrate for RCA samples.

In Fig. 6 the G-V curves for RCA cleaned Si are shown. The conductance was found to increase with increasing measurement frequency. The increase of the measured signal with voltage increase indicates increased leakage through the oxide, as often observed in MOS structures on p-Si.

For this reason, the G-V curves were corrected for the increased leakage. The resulting G-V curves at one measurement frequency, for all samples, are plotted in Fig. 7. The highest interface trap density is observed for MOS capacitors with a Si substrate hydrogenated without heating, which is manifested by the highest G-V peak. Moreover, in this case a complicated shape of the G-V curve is evident, indicating superimposed peaks. These peaks can be interpreted as more than one trap centre. The positions of the peaks at different gate voltages imply different positions, and consequently single interface traps in the bandgap.

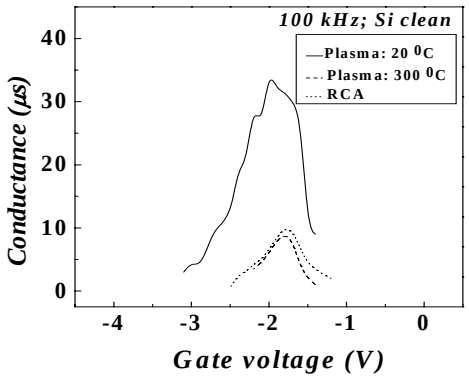

Fig. 7. G-V curves for all oxides taken at 100 kHz, corrected for the leakage through the oxide.

Comparison with the results in Fig. 1 with Fig. 2 and Fig. 4 with Fig. 5 shows that the silicon hydrogenation temperature plays an important role for the interface quality. All results, indicating reductions in the interface defect concentrations, can evidently be attributed to a thermal annealing effect.

The defect concentrations related to the fixed oxide charge has been calculated from the frequency dispersions of the *C*-V, from the difference between the experimental and theoretical flatband voltage, and the values are 1.9×10^{12} cm^{-2} ; 1.3×10^{12} cm^{-2} and 1.5×10^{12} cm^{-2} for Si-substrates preparation by hydrogenation without heating; at 300 ºC and RCA, respectively. The reduction of the fixed oxide charge is apparently due to the contribution of charge trapped in interface states.

The defect densities in this study are much smaller, on the average by 2.4 times, for all samples, in comparison to (111)Si [8], as can be expected from the known orientation dependence [9, 10]. For oxides that have not been subjected to any annealing, these densities are relatively small [11].

5. Conclusions

The electrical characterization of thin (10 nm) SiO_2, thermally grown on hydrogenated (100) silicon has revealed large interface defect densities when hydrogenation has been performed without substrate heating. This is attributed to the formation of defects on the Si surface. Increasing the temperature during hydrogenation results in lower defect densities ($1{,}3x10^{12}$ cm^{-2} for the fixed oxide charge). The reduction of the fixed oxide charge is apparently due to the contribution of charge trapped in interface states.

Acknowledgement

This work was supported by the Scientific Council, Technical University Sofia, under contract 779-10.

References

[1] The International Technology Roadmap for Semiconductors (2004).
[2] D. Bauza, Solid St. Electron., **47** 1677-1683 (2003).
[3] Dai Yue-hua, Chen Jun-ning, Ke Dao-ming, Xu Chao, Sun Jia-e, Solid St. Electron. **50**, 1472-1474 (2006).
[4] S. Alexandrova, A. Szekeres, D. Dimova- Malinovska, Solid St. Electron. **43**, 1113 (1999).
[5] S. Alexandrova, A. Szekeres, Thin Solid Films **343/344**, 385 (1999).
[6] W. Kern, RCA rev. **31**, 871 (1970).
[7] E. H. Nicollian and J. R. Brews, MOS (Metal Oxide Semiconductor) Physics and Technology, New York, Wiley (1982).
[8] S. Alexandrova, A. Szekeres, E. Halova, Physica B **308-310**, 485-488 (2001).
[9] P. K. Hurley, B. J. O'Sullivan, F N. Cubaynes, P. A. Stolk, F. P. Widdershoven, J. H. Das, J. Electrochemical Soc. **149**, G194 (2002).
[10] A. Stesmans, V. V. Afanas'ev, J. Vac. Sci. Technol. B **16**, 3108 (1998).
[11] B. J. O'Sullivan, P. K. Hurley, J. Appl. Phys. **89**, 3811-3820 (2001).

*Corresponding author: ehalova@tu-sofia.bg