JOURNAL OF OPTOELECTRONICS AND ADVANCED MATERIALS Vol. 9, No. 4, April 2007, p. 818 - 821

Electrical properties of n-Si /Cu Schottky diodes formed by electrodeposition

M. AHMETOGLU (AFRAILOV)*, M. ALPER, M. SAFAK, K. ERTURK, B. GURPINAR, F. KOCAK, C. HACIISMAILOGLU
Department of Physics, Uludag University, 16059, Görukle, Bursa, Turkey

In this paper we report the electrical characteristics of the Schottky diodes formed by electrodeposition of copper on n- Si (111) from 0.2 M $CuSO_4 \cdot 5H_2O$ + 0.5 M H_3BO_3 (pH=2.0) solution. Electrical measurements have been carried out at room temperature. n-Si /Cu diode current-voltage characteristics display low reverse- bias leakage currents and average barrier heights of 0.59 ± 0.02 eV and 0.67 ± 0.02 eV obtained from both $I-V$ and $C-V$ measurements at room temperature, respectively.

(Received November 2, 2006; accepted February 28, 2007)

Keywords: Electrodeposition, Schottky diodes, Electrical properties

1. Introduction

Interfaces between thin metal layers and semiconductors are used in optical detectors, solar cells [1] and chemical sensors [2-3]. The transport properties of such Schottky diodes and the dependence of the transport parameters on preparation are of essential importance for the device performance. Metal-semiconductor interfaces may be characterized by photoelectrical and current-voltage ($I-V$) measurements [4-5].

The metallization of semiconductor surfaces is still mostly performed in vacuum by evaporation or sputtering. The process itself is of great technological importance of Schottky barriers and ohmic contacts in electronic devices. As an alternative to the deposition from the vapor phase, many metals can be electrodeposited onto semiconductors from solution. By varying the overpotential or the composition of the electrolyte, it is possible to influence the growth mode and the structure of the deposit. Therefore it is necessary to understand in detail the mechanisms of nucleation and growth as well as the structural properties of electrodeposits.

Because of a replacement of aluminum by copper in the silicon metallization process [6], the electrochemical deposition of metals, particularly of copper on silicon has received increased interest in recent years. Despite its great industrial importance, relatively little work is reported in the literature on the fundamental aspects of electroplating on semiconductor substrates [7-9]. So far, most of the work about metal deposition onto semiconductors was performed with classical electrochemical methods.

In the following, we report on the $I-V$ and $C-V$ measurement results of the Schottky diodes formed by electrodeposition of copper on n- Si (111) from a copper sulphate bath.

2. Experimental

One-sided polished n-Si (111) samples, phosphorus-doped, 1-20 Ωcm (N_D =10^{15}cm^{-3}) were used as substrate. They were cleaned following cleaning procedure [10], which means degreasing in 2-propanol under reflux for 2 h and then boiling alternating for 15 min in basic and acidic H_2O_2 solutions. Prior to each experiment the substrates were etched for 1 min in 20% HF (Merck, VLSI Selectipur) to remove the oxide layer. Ohmic contacts were formed by vacuum evaporation of an Au layer on the back of the wafers after the etching procedure.

Copper was deposited from an electrolyte containing 0.2 M $CuSO_4 \cdot 5H_2O$ + 0.5 M H_3BO_3 (pH=2.0). The electrochemical experiments were carried out in a conventional three-electrode cell connected to a potentiostat. A saturated calomel electrode (SCE) and a platinum sheet served as reference and counter electrode, respectively. All potentials are reported versus SCE. The current-voltage (*I-V*) measurements were performed using a Keithley 2400 voltage source and capacitance-voltage measurements were carried out at room temperature with KEITHLEY 590/1M *C-V* Analyzer. All measurements were controlled by a computer via an IEEE – 488 standard interface so that the data collecting, processing and plotting could be accomplished automatically.

3. Results and discussion

The electrical characterizations of the device were achieved through I-V and C-V measurements at 300 K. The formation of a Schottky barrier between a Cu layer and n-doped Si (111) at room tempereture in shown in Fig. 1.

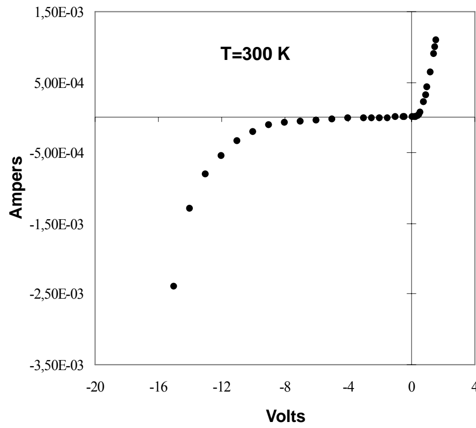

Fig. 1. The experimental forward and reverse bias current versus voltage characteristics in a linear scale of Cu/ n-Si Schottky barrier diodes at room temperature.

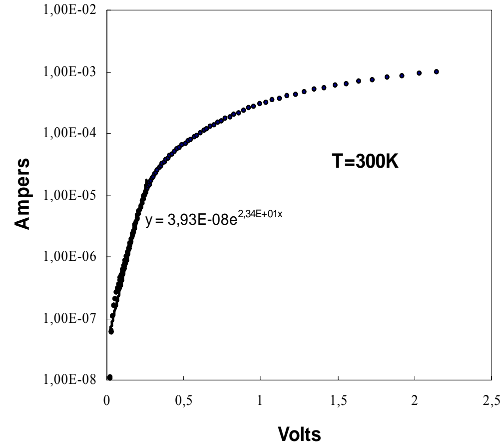

Fig. 2. The semilog - forward bias current-voltage ($I-V$) characteristics of Cu/n-Si Schottky barrier diodes at room temperature.

The reverse and forward currents of diodes demonstrate that the rectifying properties and the rectification coefficient was 108.7. The current through a Schottky barrier diode at a forward bias *V*, based on the thermionic emission theory, is given by the relation [11],

$$J = J_0 \exp\left(\frac{qV}{nkT}\right)\left[1-\exp\left(-\frac{qV}{kT}\right)\right] \tag{1}$$

where J_0 is the saturation current density is given by

$$J_0 = A^* T^2 \exp\left(-\frac{q\phi_{B0}}{kT}\right) \tag{2}$$

where q is the electron charge, V is the forward bias voltage, k is the Boltzmann constant, T is the absolute temperature, A is the effective diode area, $A^* = 4\pi q m^* k^2 / h^3$ is the effective Richardson constant of 110 A/cm^{2}K^2 for n-type Si, ϕ_{B0} is the zero bias apparent barrier height (BH) and n is the ideality factor. The saturation current density J_0 was derived by extrapolation of the linear forward part to the axis and it was found to be 5.42×10^{-4} A cm^{-2}, in agreement with the reverse bias current. The ideality factor is calculated from slope of the linear region of the forward bias $\ln J$ -V plot and can be written from Eq.(1) as:

$$n = \frac{q}{kT}\left(\frac{dV}{d(\ln J)}\right) \tag{3}$$

The zero-bias barrier height ϕ_{b0} is given by:

$$\phi_{b0} = \frac{kT}{q}\ln\left(\frac{A^* T^2}{J_0}\right) \tag{4}$$

The semilog-forward bias *I-V* characteristics of the Cu/n-Si(111) Schottky barrier diodes at room temperature is shown in Fig. 2.

The experimental values of ϕ_{B0} and n, were determined from intercepts and slopes of the forward $\ln J$ versus V plot, respectively. The experimental values of 1.62 and 0.59 ± 0.02 eV obtained for the ideality factor (n) and zero bias barrier height (ϕ_{B0}) of diodes Cu/n-Si, respectively.

The bias dependence of the reverse current, often referred to as the soft reverse characteristic, cannot be explained within thermionic emission theory across a sharp barrier using Eq.(1). It may be due to the inhomogeneous Schottky barrier which softens the reverse characteristics significantly [12]. Additionally, tunneling contacts, parellel to the Schottky diode, may be formed on thin oxide layers around the etched window during evaporation.

The capacitance-voltage ($C-V$) charac-teristics are one of the fundamental properties of the Schottky barrier diodes structure. Fig. 3 shows the capacitance-voltage characteristics taken at a temperature T=300 K and frequency f =1 MHz.

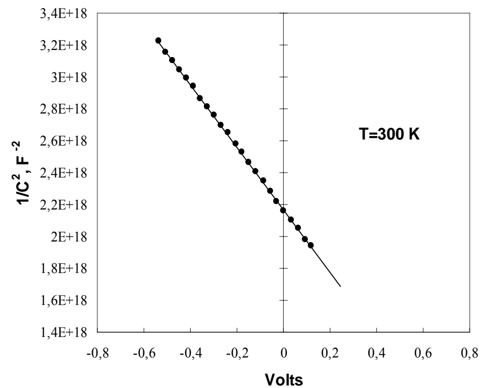

Fig. 3. The room temperature reverse bias $1/C^2 - V$ characteristics of Cu/ n-Si Schottky barrier diodes.

The characteristics are satisfactorily described by the dependence $C^{-2} \sim V$, typical of a abrupt junction. The $C-V$ dependence can be interpreted by the law,

$$\frac{1}{C^2} = \frac{2(V_R + V_B)}{q\varepsilon_S N_D A^2} \tag{5}$$

Where A, is the area of the diode, V_R the reverse bias voltage, V_B is the built in (diffusion) potential at zero bias and is determined from the extrapolation of the $1/C^2 - V$ plot to the V -axis, ε_S is the dielectric constant of the Si, q is the electronic charge and N_D is the doping concentration.

The gradient of the $C^{-2} = f(V)$ curve leads to a carrier concentration in the GaInAsSb N_d = 6,5 x 10^{14} cm^{-3}. The intercept voltage V_B in the C^{-2} vs V plots was found to be 0.39 $\pm$ 0.02 V. Once V_B is determined, the barrier height

$$\phi_{C-V} = V_B + V_n \tag{6}$$

The value of V_n can be deduced from the doping concentration as,

$$V_n = \frac{kT}{q} \ln \frac{N_C}{N_D} \tag{7}$$

Using N_d = 6,5 x 10^{14} cm^{-3} and $N_C = 2.8\text{x}10^{19}$ cm^{-3}, we obtained V_n = 0.277 V. Since the inter-cept voltage V_B is 0.39 V, the barrier height is ϕ_{C-V} =0.67 $\pm$ 0.02 V. The ϕ_{C-V} are slightly lager than the ϕ_{I-V}, this difference is explained due to an interface layer or to trap states in the substrate, the effect of the image force and barrier inhomogeneities [13].

The non-uniformity of doping at the interface should manifest itself when considering the impurity density distribution, $N(x)$ is directly proportional to the first derivative of $1/C^2$ with respect to V and is given by [14],

$$N(x) = \frac{2}{q\varepsilon_S}\left[\frac{-d\left(\frac{1}{C^2}\right)}{dV}\right]^{-1} \tag{8}$$

The above equation and relation $C = \frac{\varepsilon_S A}{W}$ are used to compute the doping profile of Fig. 4 (the majority carrier densities versus depth (W) across the depleted zone). It is seen that the impurity density distribution is very uniform with average doping concentration of N_d = 6,5 × 10^{14} cm^{-3}. No information is obtained at the interface $(x = 0)$ as is typical for doping profiles obtained from $C-V$ measurements. This is because the capacitance measurement is limited to small forward bias voltages since the forward bias current and the diffusion capacitance affect the accuracy of the capacitance measurement.

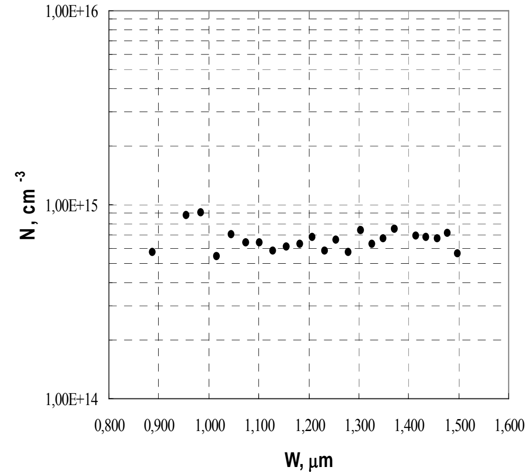

Fig. 4. Calculated doping profile obtained from $C-V$ measured data.

4. Conclusion

In this work we investigated the main electrical properties of the Schottky diodes formed by electrodeposition of copper on n- Si (111) from 0.2 M $CuSO_4 \cdot 5H_2O$ + 0.5 M H_3BO_3 (pH=2.0) solution, through the barrier heights, the ideality factors and the impurity density distribution, by using current-voltage ($I-V$) and reverse bias capacitance voltage ($C-V$) characteristics. Electrical measurements have been carried out at room temperature. The distribution density of carriers throughout Cu--/ n-Si Schottky barrier structures, derived from $C-V$ data, was used to calculate the majority carrier densities versus depth (W) across the depleted region.

Acknowledgments

This work was supported by Uludag University, Scientific Research Project Unit grant No. 2003/100. The authors would like to thank for this support.

References

[1] S. M. Sze, Physics of Semiconductor Devices, 2nd ed. Willey, New York, (1981).
[2] H. Nienhaus, H. S. Bergh, B. Gergen, A. Ma-jumdar, W. H. Weinberg, E. W. McFarland, Phys. Rev. Lett. **82**, 446 (1999).
[3] W. Göpel, K. D. Schierbaum, in Sensors, edited by W. Göpel, J. Hesse, and J.N. Zemel, VCH, Weinheim, **2**, p.429ff., (1991).
[4] B. B. Kuliev, B. Lalavich, M. Yousuf, D. M. Safarov,

Sov. Phys. Semicon. **17**, 875 (1983).
[5] M. Prietsch, Phys. Rep. **253**,163 (1995).
[6] P. C. Andricacos, Electrochem. Soc. Interface **8**, 32 (1999).
[7] G. Oskam, J. G. Long, A. Natarajan, P. C. Searson, J. Phys. D: Appl. Phys. **31,** 1927 (1998).
[8] J. C. Ziegler, G. Scherb, O. Bunk, A. Kazimirov, L. X. Cao, D. M. Kolb, R. L. Johnson, J. Zegenhagen, Surf. Sci. **452**, 150 (2000).
[9] T. Zambelli, M. L. Munford, F. Pillier, M.-C. Bernard, P. Allonque, J. Electrochem. Soc. **148**, C614 (2001).
[10] M. L. Munford, F. Maroun, R. Cortes, P. Allonque, A. A. Pasa, Surf. Sci. **537**, 95 (2003).
[11] E. H. Rhoderick, R. H. Williams, Metal-Semiconductor Contacts, Clarendon Press, Oxford . (1988).
[12] J. P. Sullivan, R. T. Tung, M. R. Pinto, W. R. Graham, J. Appl. Phys. **70**, 7403 (1991).
[13] M. Siad, A. Keffous, S. Mama, Y. Belkacem, H. Menari, Appl. Surf. Sci. **236**, 366 (2004).
[14] H. Kroemer, Appl. Phys. Lett. **46**, 504 (1985).

*Corresponding author: afrailov@uludag.edu.tr