Electro-optical cyclic redundancy check error decoder using lithium niobate based Mach-Zehnder interferometer

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Error detection using optical parity generation has emerged as an evolving area of research in the field of optical communication networks. This paper presents the popular forward error correction technique of cyclic redundancy check (CRC) code words using the electro-optical method. CRC has served as a dominant technique to tackle multiple bit errors that occur in bursts. The structure has been designed using LiNbO$_3$ based Mach-Zehnder Interferometer. Critical parameters such as extinction ratio (38.59 dB), insertion loss (0.043 dB), and contrast ratio (22.54 dB) have been computed and shown in the paper.

1. Introduction

With the increase in the demand for high data transmission rates and large capacity channels, the need for optical signal processing networks has increased drastically. Optical communication networks provide a viable solution to fulfill the users' needs of large bandwidth [1], [2]. But the losses in the channel adds to the probability of errors in the channel. The error probability cannot be made zero, but techniques can be applied to minimize it. Several coding techniques are used in application to identify and remove the erroneous bits. The evolution of error coding techniques can be traced back to the 1950s, when R.W. Hamming designed the well-known Hamming codes [3]. All forms of error coding techniques require the addition of extra parity bits at a suitable position(s) in the code for easy decoding of the erroneous word. The fundamentals of both, parity generation and checking involve XORing of the input bits [4]–[6]. Researchers have successfully achieved parity generation and checking using various optical techniques - Terahertz Optical Asymmetric Demultiplexer (TOAD) switch [7], Micro Ring Resonator (MRR) [8], Semiconductor Optical Amplified – Mach-Zehnder Interferometer (SOA-MZI) [9], Quantum Dot SOA (QD-SOA) [10], SOA-assisted Sagnac Interferometer [11], Metal–Polymer–Silicon Hybrid Plasmonic Waveguide Mach-Zehnder switch [12], lithium niobate based Mach-Zehnder Interferometer (LN-MZI)[13]–[15], non-linear MZI switch [16], and Metal-insulator-metal based plasmonic Mach-Zehnder Interferometer (P-MZI) [17].

In 1999, Poustie *et al.* formulated a complex design for an all-optical parity checker with bit-differential delay using TOAD switches. Increased latency due to the differential delay becomes a major drawback of the design [18]. In 2009, Wang *et al.* also demonstrated an all-optical

TOAD based XOR gate and reported an extinction ratio (ER) of 13.29 dB [7]. Rakshit *et al.* employed a microring resonator to design an all-optical 3-bit generator and checker circuit obtaining an ER of 12.1 dB [8].

All these works like most of the others available in the literature have reported a single bit parity detection, without considering any dedicated error control method. Our group has been committed to potent error detection/ correction techniques and have reported works such as Hamming code [19], [20], linear block code [21], [22], convolutional code [23]. In the digital electronic domain, these techniques are well established and have been extensively used for the identification of error locations and their corrections, respectively. Our group has proposed these methodologies for the optical domain with all the designs based on multiple LN-MZI switches cascaded to produce multiple parity bits. While all these works have one common objective of error detection and providing the location of the error in the received code at the receiver end and / or generation of these codes at the transmission end. All these designs differ from each other in the methodology of error detection and location identification.

The authors propose here an electro-optical (EO) circuit for the implementation of (7, 4) cyclic redundancy check (CRC) error detection. CRC is a subclass of linear block codes that provides a simple and easy implementation of the encoder and the decoder circuit. For a cyclic code, a lateral shift in the code produces another valid code. CRC offers a powerful error detection scheme which enables an easier way to detect errors that occur in bursts [4], [5]. A (7, 4) CRC code word has a polynomial length of three. The code has a minimum Hamming distance of three and has a capacity of correcting all single-bit errors. A theoretical review of CRC encoding and decoding is given in Section 3. CRC codes are

primarily applied in local area networks and wide area networks [5]. Some of the major applications of CRC are shown in Table 1.

Lithium niobate has been a favourable contender for designing the optical switches using Mach-Zehnder Interferometer. It has extensively been used in integrated optics and guided wave optics. Lithium niobate is a man-made ferroelectric material that has been used for a variety of applications due to its excellent properties such as high electro-optic coefficient, large birefringence, piezoelectric effect, pyroelectric effect, and many others. It has a large electro-optic coefficient, r_{33} of 30.8×10^{-12} m/V which enables switching at very low voltages (0V and 6.75V) [13]–[15], [24]–[31].

Table 1. Some of the commonly used CRC codes with applications

CRC Code	Applications	Polynomial Length
CRC-4	ITU G.704	5
CRC-8	ATM HEADER	8
CRC-10	ATM AAL	11
CRC-16	BLUETOOTH	17
CRC-32	LANs	33

The paper has been organized into sections. Section 2 explains the operating principle; Section 3 provides the necessary theoretical background of the CRC codes; Section 4 discusses the proposed design along with its analysis and implementation using the LN-MZI based optical switch; in the end Section 5 provides a critical conclusion to this study.

2. Principle of operation

The Mach-Zehnder Interferometer employed in the proposed design is based on the linear electro-optic effect exhibited by lithium niobate. A 1 mW continuous wave (CW) applied at the input port of the EO switch experiences a phase shift depending upon the potential difference applied across the electrodes. The central electrode is applied with the data bit while the other two electrodes are kept at ground. Data bit '1' (6.75V) introduces a zero phase shift leading the CW to the bar port while the bit '0' (0V) presents a phase shift of π rad forcing the output to the cross port [13]. The operation of a Ti: LiNbO₃ based Mach-Zehnder Interferometer can be understood with the help of Fig. 1.
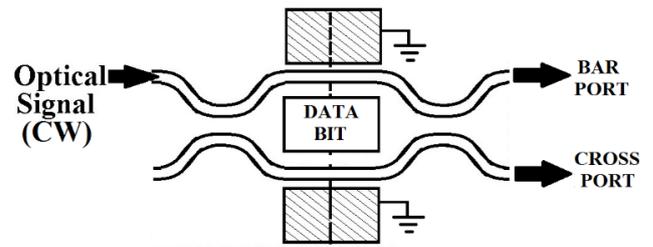
Fig. 1. Ti: LiNbO₃ based Mach-Zehnder interferometer

Power at the output ports are expressed in normalized form as [15], [21]:

$$\text{Bar port: } P_{BAR} = \sin^2(\Delta\Phi/2) \tag{1}$$

$$\text{Cross port: } P_{CROSS} = \cos^2(\Delta\Phi/2) \tag{2}$$

where $\Delta\Phi$ represents the phase difference between the input and the output port of the LN-MZI.

Table 2 lists some of the major design parameters used in the designing of a single LN-MZI.

Table 2. Design parameters of single LN-MZI

Parameter	Value
Crystal material Crystal cut, Propagation direction	LiNbO₃ Z-cut, Y-axis
Waveguide material Extra-ordinary electro-optic coefficient (r_e) Length (L) of EO material	Ti: LiNbO₃ 30.8 x 10⁻¹² m/V 10,000 µm
Dielectric Material	Air (RI=1.00)
Cladding	Air
Substrate	LiNbO₃ (RI=2.23)
Polarization, Input Optical Power (CW)	Modal, 1mW

3. Review of cyclic redundancy check

An (n, k) CRC code is an n-bit code word with k data bits and (n-k) parity bits attained using a generator polynomial. For a (7, 4) CRC code the generator polynomial is derived by factorizing the polynomial $x^7 + 1$ as follows [6]:

$$x^7 + 1 = (x+1)(x^3 + x + 1)(x^3 + x^2 + 1) \tag{3}$$

where '+' denotes modulo-2 addition.

The factorization suggests two generator polynomials: $G(x) = (x^3 + x + 1)$ which is equivalent to 1011 and $(x^3 + x^2 + 1)$ equivalent to 1101. For a k-bit long data

word $D(x)$, the (n-k) parity bits are calculated by dividing the expression $x^{n-k}D(x)$ by the generator polynomial $G(x)$. The designed code word $C(x)$ is transmitted through the channel. For the received code word $R(x)$ ($R_6R_5R_4R_3R_2R_1R_0$) contaminated by error $E(x)$, a decoding scheme can be formulated to generate the desired syndrome $S(x)$ ($S_2S_1S_0$). The syndrome value is symbolic of the error position. The presented work is based on the following decoding principles.

$$R(x) = C(x) + E(x) \tag{4}$$

$$S(x) = \operatorname{Re} m \frac{R(x)}{G(x)} = \operatorname{Re} m \frac{C(x) + E(x)}{G(x)} \tag{5}$$

For an error-free code word, $C(x)$ is a multiple of $G(x)$, hence it is evenly divisible by $G(x)$.

$$S(x) = \operatorname{Re} m \frac{E(x)}{G(x)} \tag{6}$$

Logic design of the CRC decoder circuit obtained through the decoding principles is shown in Fig. 2.
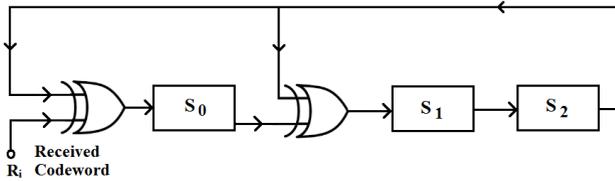
Fig. 2. (7, 4) CRC decoder logic diagram
for generator polynomial $G(x) = 1011$

The sequential logic circuit comprises a 3-bit shift register and two XOR logic gates. Bit S_1 and S_0 are obtained through modulo-2 addition, which can be performed using XOR gates. Bit S_1 is passed on to S_2 at every clock pulse.

Table 3. Calculation of 3-bit syndrome through 7 clock pulses

Pulse Cycle	Received Code Bit	Syndrome Bits		
N	R_i	$S_{2, n =}$ $S_{1, n-1}$	$S_{1, n} = S_{2,}$ $_{n-1} + S_{0, n-1}$	$S_{0, n} = R_i$ $+ S_{2, n-1}$
0	-	0	0	0
1	1	0	0	1
2	0	0	1	0
3	0	1	0	0
4	0	0	1	1
5	0	1	1	0
6	1	1	1	0
7	0	1	1	1
		S_2	S_1	S_0

The 7-bit code is input to the decoder serially in seven clock pulses, starting with the most significant bit R_6. The

shift register is initially cleared and regularly updates its contents on every cycle. The final syndrome is generated at the end of the seventh clock pulse which can be read and the erroneous word can be corrected. For the 7-bit code **'1000010'** (chosen arbitrarily) the syndrome calculation procedure has been described in detail in Table 3.

The above process generates a unique 3-bit syndrome which indicates the error position in the received code word. The erroneous position can be found using the look-up table (Table 4).

The method discussed above has been described for a 4-bit data word, which is encoded into a (7, 4) code word by adding 3-bits as parity.

Table 4. Syndrome look-up table

Syndrome			Error Position
S_2	S_1	S_0	
0	0	0	No Error
1	0	1	R_6
1	1	1	R_5
0	1	1	R_4
1	1	0	R_3
0	0	1	R_2
0	1	0	R_1
1	0	0	R_0

In case of an 8-bit data word, it can be fragmented into two 4-bit data words and then encoded to two different (7, 4) code words. At the receiver end, the two 7-bit code words need to be scrutinized separately and the 4-bit information shall be extracted. The two 4-bit data words have to be merged to gather the original 8-bit transmitted data word.

4. Electro-optical design of CRC decoder

Centred on the switch design presented in Section 2, the LN-MZI based EO design of the (7, 4) CRC decoder logic has been shown in Fig. 3. A CW is applied at the first input terminals of $V_{CRC}1$ and $V_{CRC}3$. The EO circuit consists of 2-bit optical modulo-2 adders producing the two syndrome bits S_0 and S_1. Modulo-2 adders have been designed by simply cascading two LN-MZIs. Bit S_2 is identical to S_1 in the previous cycle so it can be gained using a unit delay element as shown in Fig. 3.
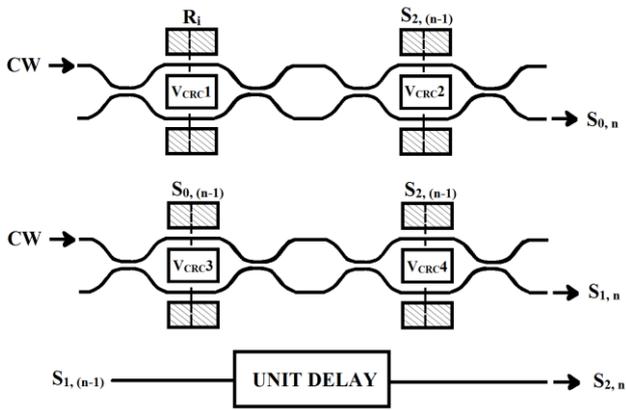
Fig. 3. Electro-optical design for LN-MZI based CRC decoder circuit

A mathematical model for the proposed design can be expressed in terms of the normalized power at the output ports.

$$P_{S_0} = \cos^2 \frac{\Delta\varphi_{V_{CRC}1}}{2}\sin^2 \frac{\Delta\varphi_{V_{CRC}2}}{2} + \sin^2 \frac{\Delta\varphi_{V_{CRC}1}}{2}\cos^2 \frac{\Delta\varphi_{V_{CRC}2}}{2} \quad (7)$$

$$P_{S_1} = \cos^2 \frac{\Delta\varphi_{V_{CRC}3}}{2}\sin^2 \frac{\Delta\varphi_{V_{CRC}4}}{2} + \sin^2 \frac{\Delta\varphi_{V_{CRC}3}}{2}\cos^2 \frac{\Delta\varphi_{V_{CRC}4}}{2} \quad (8)$$

The above equations can be minimized as:

$$P_{S_0} = \frac{1}{2}\left[\sin^2\left(\frac{\Delta\varphi_{V_{CRC}1} + \Delta\varphi_{V_{CRC}2}}{2}\right) + \sin^2\left(\frac{\Delta\varphi_{V_{CRC}1} - \Delta\varphi_{V_{CRC}2}}{2}\right)\right] \quad (9)$$

$$P_{S_1} = \frac{1}{2}\left[\sin^2\left(\frac{\Delta\varphi_{V_{CRC}3} + \Delta\varphi_{V_{CRC}4}}{2}\right) + \sin^2\left(\frac{\Delta\varphi_{V_{CRC}3} - \Delta\varphi_{V_{CRC}4}}{2}\right)\right] \quad (10)$$

The normalized power of output S_2 will be the same as derived for the output S_1.

4.1. Opti-BPM Implementation of (7, 4) CRC Decoder

A detailed analysis of the optical CRC decoder circuit is presented in this section. Among the 2^7 possible cases of received code words, one case of a transmitted code word is discussed further to exhibit the functionality of the proposed device. Table 3 shows the variation of the syndrome bits stored in the 3-bit shift register at every clock cycle. After 7 pulses the final syndrome is obtained which indicates the erroneous bit position. The CRC decoder proposed has been tested against the theoretical results of Table 3 using Opti-BPM (Fig. 3). The code '1000010' (Table 3) has been tested which contains an error at the bit R_5.

The design suggested in Fig. 3 is simulated using Opti-BPM software, under transparent boundary conditions using the 2D paraxial beam propagation method (BPM). A finite-difference engine with a propagation step of 1.3 containing a mesh of 8.33 points/µm is employed. At the inputs, TM polarized continuous wave of 1.3µm has been applied at the first input port. Fig. 4 shows the BPM implementation of the CRC decoder considering 1-bit errors in the received code words.
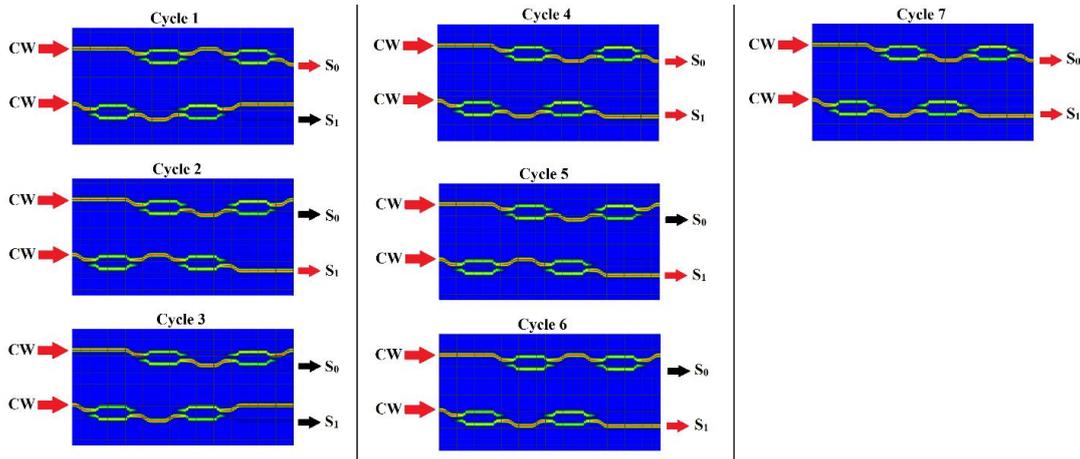
Fig. 4. Opti- BPM simulation of (7, 4) CRC decoder for received code word = 1000010, $S_2S_1S_0$ = 111, error at R_5 (color online)

The results presented in Table 3 and Fig. 4 are wholly in agreement with each other. Two syndrome bits S_1 and S_0 have been derived above. Bit S_2 has not been considered in the simulation as it can be derived from the value of bit S_1 in the previous cycle. Cycle 7 reports the final S_1 and S_0 values as 11. The above results indicate the syndrome word as $S_2S_1S_0$=111, suggesting the received code word to be contaminated at bit R_5 (Table 4).

Results projected in Fig. 5 illustrate the variation of the optical field and refractive index at the output plane. It can be seen in the different cases of the simulation that the power at logic '0' output is not zero but finite. This occurs due to the coupling between the output waveguides which leaks the power from one port to the other. Due to this the extinction ratio of the device gets affected.
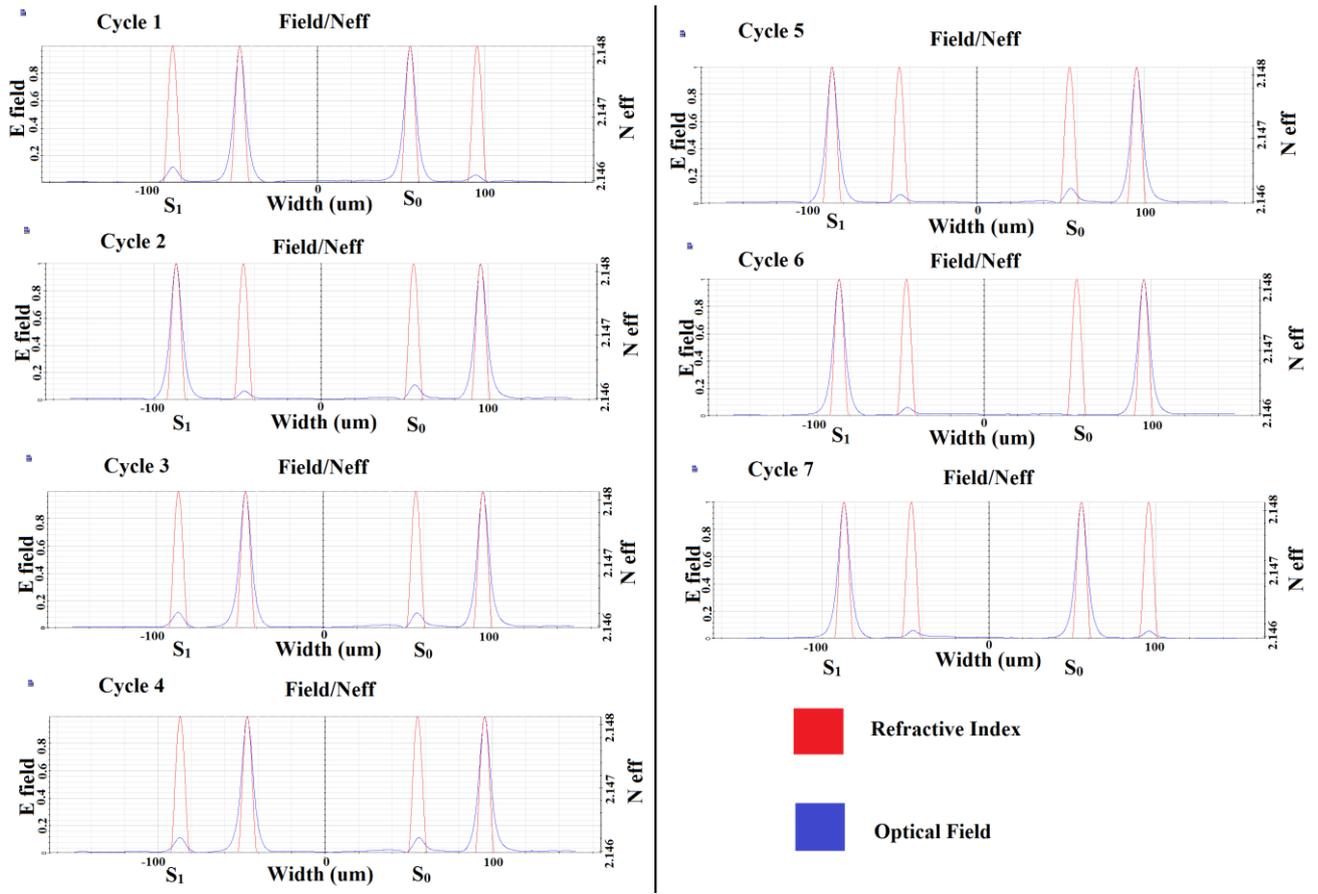
Fig. 5. Variation of optical field and refractive index at the output plane (color online)

Table 5. Performance analysis of the proposed device

Sr. No.	Parameter	Formula Used	Calculated Value (dB)	Desirable Value (dB)
1	Extinction Ratio	$10\log_{10}\left(\dfrac{P_{ON}}{P_{OFF}}\right)$ (P_{ON} - output power in ON state, P_{OFF} - output power in OFF state)	18.53 - 38.59	> 15 dB
2	Insertion Loss	$10\log_{10}\left(\dfrac{P_{out}}{P_{in}}\right)$ (P_{out} - output power, P_{in} - input power)	0.043	< 1 dB
3	Contrast Ratio	$10\log_{10}\left(\dfrac{P_{1Mean}}{P_{0Mean}}\right)$ ($P^{1}{}_{Mean}$ - mean output power for logic output 1 $P^{0}{}_{Mean}$ - mean output power for logic output 0)	22.54	> 20 dB

4.2. CRC decoder analysis

Optical circuits can be evaluated based on performance factors such as extinction ratio, contrast ratio (CR), and insertion loss (IL). For an ON-OFF switch, ER is described as the ratio of the output power in the ON state to the output power in the OFF state [13], [15]. LN-MZI here is being used as an external modulator so it becomes very important for this factor to be as high as possible. In general, high-speed optical switches have ER > 15 dB [13], [15]. Contrast ratio gives the ratio of the mean powers in the ON and OFF states. Considering the mean of the powers it covers the overall performance of the switch [8]. Its value is required to be high (>20 dB) for

maximum transfer of power. Insertion loss value gives an idea of the measure of the input power that is lost in the operation. A fast performance switch is expected to have an insertion loss value as low as possible [15].

Table 5 presents the performance analysis of the simulated design on the basis of the defined critical performance parameters.

5. Conclusion

The cyclic redundancy check code built on the electro-optical scheme has been simulated and studied using the beam propagation method effectively in the present work. CRC is one of the most powerful techniques of burst error detection. The scheme here demonstrates the adequate operation of the checker using the proposed implementation. The structure has three outputs S_2, S_1, and S_0 where S_2 is the unit delayed version of S_1. Derivation of the output S_1 and S_0 is shown with the help of modulo-2 adders. S_2 is assumed to be derived from the S_1 value in the preceding cycle. The presented scheme can be extended and employed for decoding of higher lengths of code words by splitting it into smaller lengths. The extinction ratio value shows an average of about 28.56 dB varying in the range 18.53 - 38.59 dB which indicates a respectable performance of the device. The contrast ratio is also reported with a decent value of 22.54 dB. Also, the calculated insertion loss value of 0.043 dB suggests a low power loss in the operation. Obtained ER, CR, and IL values advocate a healthy performance of the device.

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