Fabrication of antireflective silicon nanowires array

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In this work, vertical aligned SiNWs array have been fabricated on silicon wafers via metal assisted chemical etching method. This method mainly contains four fabrication steps: wafer cleaning, oxide layer removal, silver catalyst deposition and metal assisted etching. The relationship between the etching time and nanowires length is investigated, and the nanowires can be fabricated in a controllable manner. The optical characteristic of the nanowires array is measured. The average optical reflectance of the SiNWs array is as low as about 3.28% when the etching time is 20 min, implying such prepared SiNWs array possesses an excellent antireflective property. The successful transfer of the SiNWs array from the rigid silicon substrate onto a flexible PDMS film demonstrates its potential in fabricating flexible optoelectronic devices.

1. Introduction

Due to the size effect, nanowires show a lot of special optical [1], mechanical [2] and electrical properties [3]. As a result, they have attracted widespread attention and become an important research focus in nanomaterials. Among the widely studied nanowires including ZnO nanowires [4, 5], silicon nanowire wires (SiNWs) [6], silicon oxide nanowires [7], CdS nanowires [8, 9], SiNWs are particularly interesting since they are non-toxic and compatible with major silicon-based microelectronic devices.

SiNWs can be used in many fields, such as solar cell [10], lithium ion battery [11], sensor [12], laser [13] etc. Specially, the SiNWs array can be fabricated into low-cost and high-efficiency solar cells compared to traditional bulk silicon based solar cells. They can absorb much more light and separate electron-hole pairs more effectively [14]. There are a variety of methods to synthesize SiNWs including bottom-up approaches: vapor-liquid-solid (VLS) growth [15] and hydrothermal [16]. Metal assisted chemical etching (MACE) is another very promising top-down process discovered recently for the synthesis of SiNWs [17-20]. In this work, we demonstrate the fabrication of vertical aligned SiNWs arrays with MACE. The etching process is researched systematically, and SiNWs array with a very low optical reflectance is obtained. Traditionally, the SiNWs are fabricated on rigid silicon substrate [20]. This greatly restricts their application. Here, we have transferred the SiNWs array successfully from the rigid silicon substrate to a flexible substrate, which is a key step for fabricating flexible optoelectronic devices.

2. Experimental

P-type, 1-10Ω·cm, Si (100) wafers were used for MACE. The fabrication procedure is illustrated schematically in Fig.1. First, the silicon wafer was sequentially cleaned with acetone, DI water and piranha solution for 10 min (H_2SO_4 (97%):H_2O_2 (30%) = 3:1 by volume) to remove the organic and inorganic impurities on the surfaces of silicon wafers. Next, in order to remove the native oxide layer and increase the activity of the silicon surface, the silicon wafers were rinsed with diluted HF solution (5%) for 5 min. Then the wafers were immersed into a mixed solution containing 5.0M HF and 0.01M $AgNO_3$ for 1 min to deposit a porous Ag film onto the wafer surface. The Ag film acted as catalyst for Si etching. The etching was carried out in a solution containing 5.0M HF and 0.5M H_2O_2, so as to obtain SiNWs arrays on the silicon substrate. Finally, the samples were immersed into concentrated nitric acid (69%) for 3 min and rinsed with DI water to remove the residual Ag catalyst.
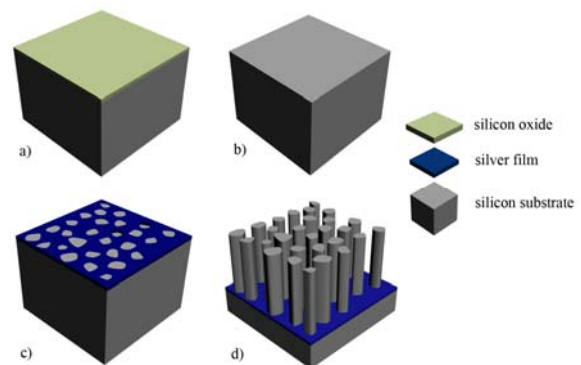

Fig.1. The process steps for fabrication of SiNWs array, (a) cleaning the wafer (b) removing the oxide layer (c) depositing a silver film (d) metal assisted etching.
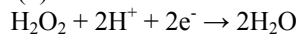
The morphology of the prepared SiNWs was characterized using scanning electron microscopy (SEM). After that, the SiNWs were diluted in ethanol, transferred to carbon grid, and characterized using transmission electron microscopy (TEM).
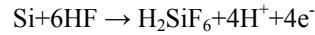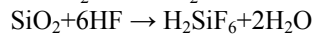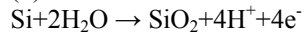
3. Results and discussion

3.1. Mechanism

In the experiments, a porous silver film is deposited onto the surface of silicon wafers by galvanic displacement reaction, and two half-cell reactions including cathode and anode reactions take place [21]. Here, the silver facing the etching solution acts as the cathode and the other side of the silver facing the silicon acts as anode. The anode consumes the silicon substrate continuously, making the etching proceeding. The reactions on the cathode and anode are listed as follows.
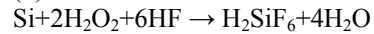
(1) Cathode:
$$H_2O_2 + 2H^+ + 2e^- \rightarrow 2H_2O$$
(2) Anode:
$$Si+2H_2O \rightarrow SiO_2+4H^++4e^-$$
$$SiO_2+6HF \rightarrow H_2SiF_6+2H_2O$$

$$Si+6HF \rightarrow H_2SiF_6+4H^++4e^-$$
(3) Overall:
$$Si+2H_2O_2+6HF \rightarrow H_2SiF_6+4H_2O$$

During the etching process, the silicon beneath the silver is transformed to H_2SiF_6 and then dissolved into the etching solution.

3.2. Morphology

The morphology of SiNWs arrays is shown in Fig.2. Because of the Van der Waals forces, the SiNWs tend to agglomerate at their tips, forming bundles as shown in Fig.2a. Fig.2b is the TEM result of a silicon nanowire with the diameter less than 100 nm. Fig.2c is the HRTEM result, indicating that the silicon nanowire is a single crystal and the axis direction is [100] crystal orientation.

The cross-section images of the SiNWs arrays etched under different time duration are depicted in Fig.3, revealing that the SiNWs are vertically aligned on the Si (100) wafer. Also, the length of the nanowires could be effectively controlled by tuning the etching time. The diameter of the nanowire ranges from 50nm to 300nm. Moreover, the SiNWs can be tuned by selecting the crystal orientation and doping type of the silicon substrate, which will be studied further.
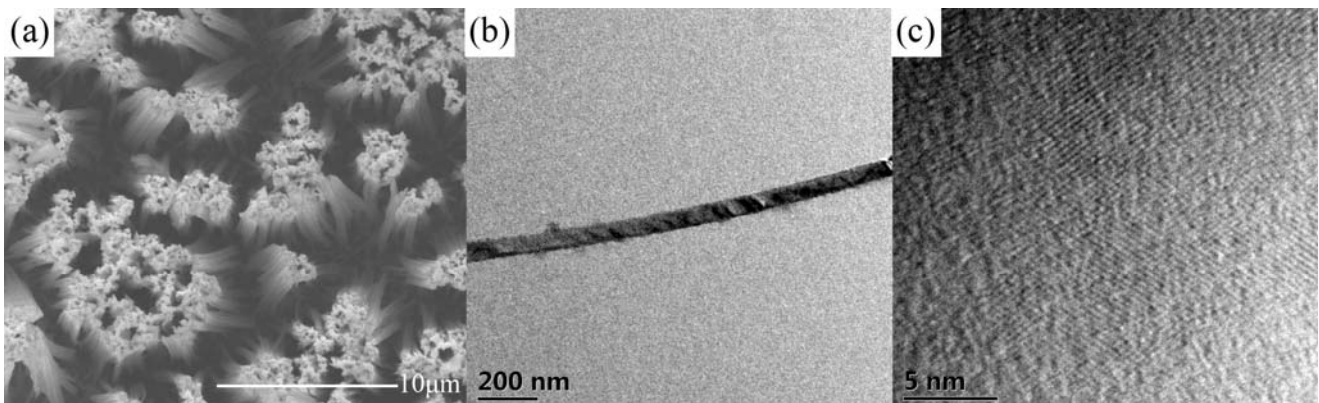

Fig.2. (a) SEM picture, top-view of the SiNWs array with etching time 20 min. (b) TEM picture of a SiNW. (c) High resolution picture.

3.3. Etching rate

The etching rate of the SiNWs array, i.e. the nanowire length as a function of the time, is shown in Fig.4. The etching rate is about 1μm/min in the beginning of the etch process. Then it slows down and reaches a plateau after about 50 min. The reason for this phenomenon may be that as the nanowires getting longer it becomes more difficult for the fresh etching solution to reach the bottom

of the SiNWs array. The exhausting of the etching byproducts may also contribute to this phenomenon. Besides, we find that as the etching time getting longer, the bottom of the SiNWs array is subjected to being broken and the tip of the SiNWs array is subjected to more serious agglomeration, deteriorating the structural integrity of the SiNWs array.
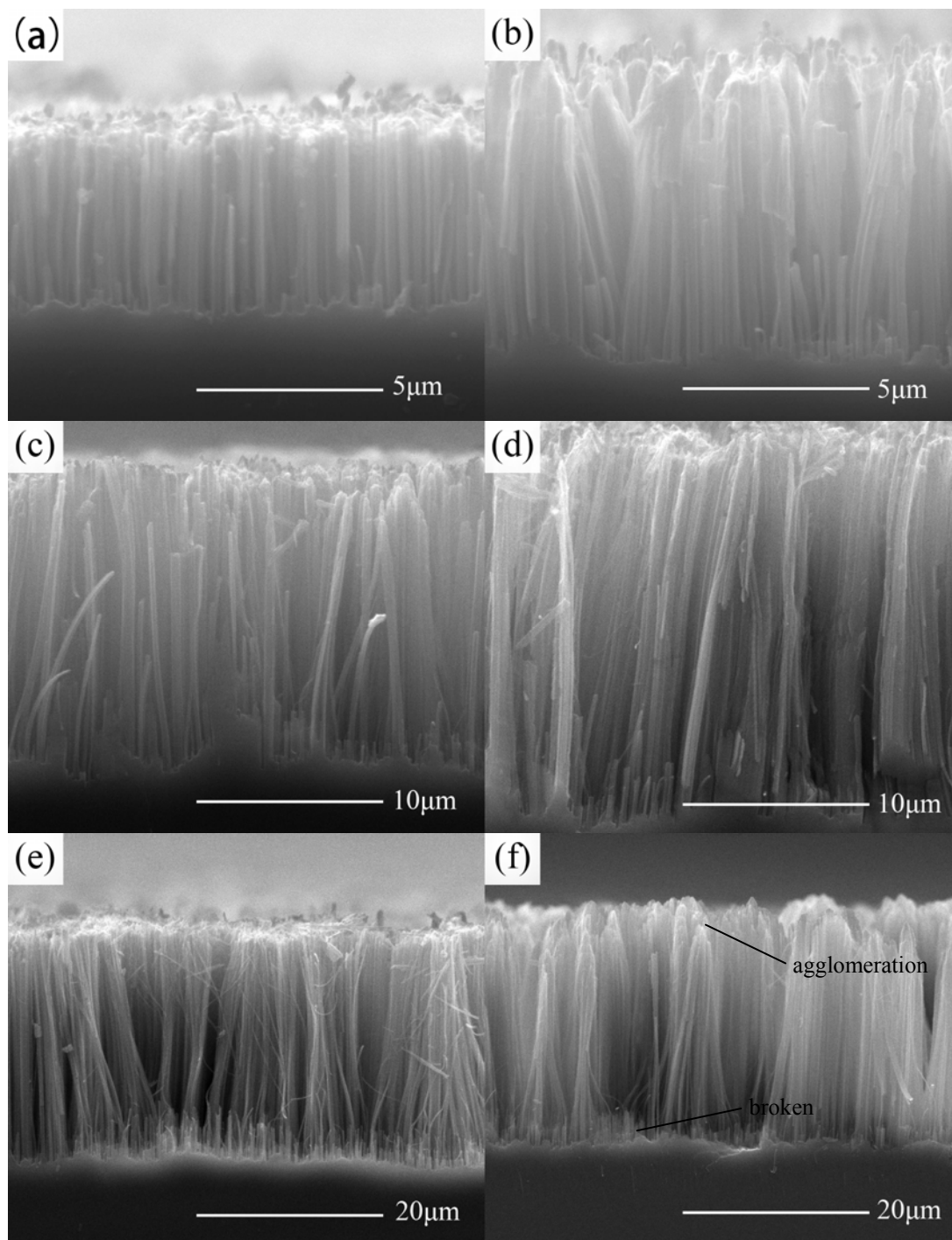
Fig.3. SEM results for the side-view of the SiNWs under different etching time. For (a), (b), (c), (d), (e) and (f), the etching time is 5 min, 10 min, 20 min, 30 min, 40 min and 50 min, respectively.
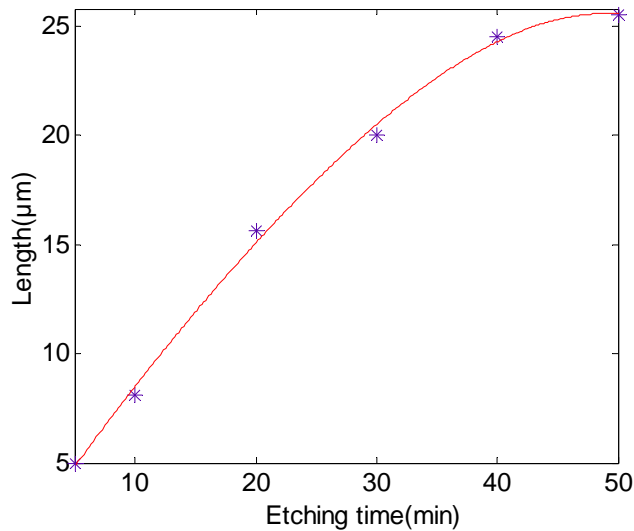
Fig.4. The relationship of the nanowires length vs. etching time (the curve is obtained with polynomial fit).

D. Optical characterization

The optical reflection of the SiNWs array fabricated with various etching time is measured using a Lambda 35 UV/VIS spectrophotometer with an integrated sphere. The results are shown in Fig.5. The range of the wavelength is 380-1100nm corresponding to the major spectral irradiance of sunlight. It can be found that there is a terrace around 400nm in the curve. Then, the reflectance gradually increases with increasing wavelength. The average reflectance of the SiNWs array under different etching time is shown in the inset. We note that the averaged optical reflectance of the SiNWs array etched under 20 min is the lowest among all SiNWs arrays under different etching time, with an average optical reflectance about 3.28%. The reason may be that the excessive etching beyond 20 min has degraded the structural integrity by weakening the bottom of the SiNWs and aggravating the agglomeration of the SiNWs, as discussed in Fig. 3.

Many kinds of antireflective structure have been developed recently. Peng Jiang's group fabricated inverted pyramid arrays as the antireflective structure. At the wavelength above 550nm the reflectance remains about 10% and the lowest point is about 2% [22]. Rui Jia's group prepared SiNWs on pyramid-array-texturing c-Si surface for the application of solar cells. The reflectance at the wavelength of 800 nm is less than 2% [23]. Jae Su Yu's group fabricated AZO/Si shell/core SWG structure which exhibited a low average reflectance of ~2% over a wide wavelength range [24]. Therefore, the antireflective characteristic of the prepared SiNWs is comparative, and the antireflective subwavelength SiNWs structure can be used in the future to improve the performance of optical and optoelectronic devices including solar cells [25], photodetectors [26], and displays [27, 28].
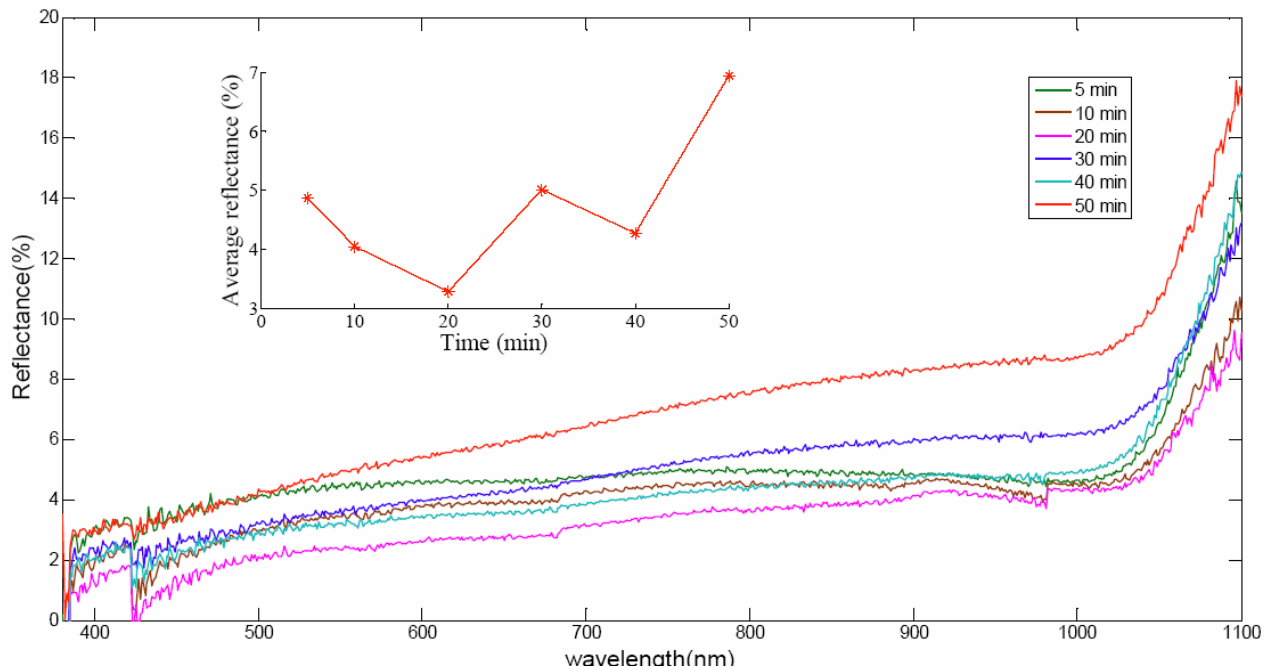

Fig.5. The optical reflectance of the SiNWs array with different etching time. The inset is the average reflectance with different etching time.

E. Transfer

Although uniform and vertical aligned SiNWs array have been fabricated, they are attached to the rigid thick bulk silicon substrate. Separating the SiNWs array from the substrate while maintaining their vertical structure will be very useful for the application of flexible optoelectronic device such as flexible solar cells. We have explored the transfer of the fabricated SiNWs array to flexible, optically transparent, polydimethylsiloxane (PDMS) film from the silicon substrate. In the experiments, a layer of PDMS solution is spin-coated onto the sample and subsequently cured. The SiNWs array is imbedded into the flexible

PDMS film and then peeled off from the substrate, mechanically assisted with a blade. As shown in Fig.6, the SiNWs array is transferred and partially imbedded in the flexible, transparent, mechanically and chemically robust PDMS film. The inset is an optical picture (taken by KEYENCE VHX-1000) of the side-view of the SiNWs array imbedded in PDMS. The SiNWs array transferred onto the PDMS film maintains the spacing, morphology, and orientation of the SiNWs array prior to the transfer. In addition, the silicon substrate can be used again for the fabrication of SiNWs array after polishing process such as chemical mechanical polishing.
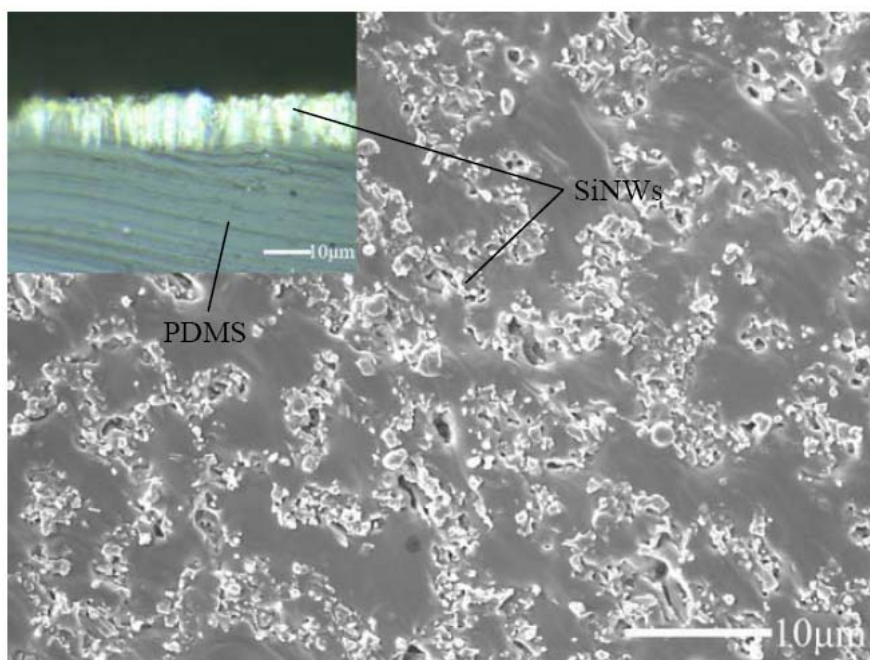

Fig.6. SEM picture of the SiNWs array embedded in PDMS.
The inset is the optical picture of the side-view of the SiNWs array.

4. Conclusions

Vertical aligned SiNWs array has been fabricated by metal assisted chemical etching method. Our fabrication process demonstrates that the silicon nanowires array can be formed at the etching rate about 1μm/min in the beginning, and then the rate decreases with increasing etching time. As a result, the length of the silicon nanowire can be tuned by adjusting the etching time. The obtained SiNWs array possesses very good antireflective performance, and we have achieved an average optical reflectance of the SiNWs array as low as about 3.28% under 20 min etching time.

Because the solid, rigid silicon substrate restricts the application of the SiNWs array, we have separated the silicon nanowire array from the substrate and transferred them onto a flexible PDMS substrate, which can be used in flexible optoelectronic devices in the future.

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