Fabrication of n-i-p diode using hot wire chemical vapor deposition technique

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The hetero junction with intrinsic thin layer technique shows promising advancement in the development of optoelectronics devices. In this article, we have described the fabrication and characterization of n-i-p structure hetero junction with intrinsic silicon thin layer diode on glass substrate using hot wire chemical vapour deposition technique. We have grown the device structure starting from bottom i) n-type microcrystalline silicon layer on fluorine doped tin oxide coated glass at 350°C substrate temperature, ii) intrinsic polycrystalline silicon layer at 600°C substrate temperature, iii) hydrogenated amorphous intrinsic silicon layer (a-Si:H) at 200°C substrate temperature and iv) p type amorphous silicon layer at 200°C substrate temperature on the top. FTO and aluminium were used as back and top contacts respectively. From dark current-voltage and capacitance-voltage measurement, we observed that the device had diode-like characteristics. However, further optimization of the device is needed for successful application in sensors, detectors and photovoltaic applications.

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1. Introduction

The growth of thin silicon film on glass for optoelectronics devices can become an economic solution in decreasing the dependency on silicon wafer. There has been interest in fabricating silicon structures on non-crystalline substrates such as glass. This was considered particularly important before the advent of modern crystalline silicon based technology became economical. Glass substrate requires low temperature (~400°C) procedure which is not offered by available fabrication procedures except hot wire chemical vapour deposition (HWCVD) technique [1] and plasma enhanced chemical vapour deposition technique (PECVD) [2], [3]. PECVD based deposition of silicon is widely used. Though HWCVD technique is regarded as high filament temperature (1600°C~2000°C) process but the substrate can be kept at low temperature (200°C). This feature makes HWCVD compatible with PECVD in thin film optoelectronics device such as image sensor and solar cell fabrication [4]. In the recent years (2009-2017), HWCVD grown devices have shown excellent alternative route to enhance the performance of optoelectronics devices. Low substrate temperature (~200°C) [5], thin layer (~10nm) [6], high deposition rate (~7.3nm/s) [7] and low cost solar cell (0.08euro/Wp) [8] are the key parameters in enhancement of the device performance. These optoelectronics devices have various structures but the generalised form is a p-n junction diode with metal contacts. Another version of the diode for photonic application is n-i-p structure [9]. This unique structure has proven its worthiness in the field of photo sensors [10], temperature sensors [11], biomedical sensors [12], antenna applications [13], solar cell [14] and so on. This structure is being utilized in the field of second generation solar cells with hetero junction intrinsic thin layer (HIT) with an efficiency of 23% [15], [16], where the highest is 26.7% by Kaneka corporation Japan, as given in the solar cell efficiency table-56 [17] and best research solar cell graph prepared by National Renewable Energy Laboratory (NREL). In the HIT structure, thin hydrogenated intrinsic amorphous silicon layer act as good surface passivators of crystalline silicon [18] which plays an important role in increasing the open circuit voltage [19].

In this article, we have discussed the process of fabricating HWCVD process based thin film device structure including bottom, i) n-type microcrystalline silicon layer on fluorine doped tin oxide (FTO) coated glass, ii) polycrystalline intrinsic silicon layer, iii) hydrogenated amorphous intrinsic silicon layer (a-Si:H), iv) p type a-Si:H layer and v) aluminium dot as the top contact. The dark current-voltage (I-V) and capacitance-voltage (C-V) characteristics were measured.

2. Experimental

The device fabrication initiated with the deposition of n-type phosphorous doped microcrystalline silicon thin film of 150 nm on FTO coated glass (1.5cm×2.5cm) at 350°C substrate temperature in a HWCVD system using silane and phosphine [5]. The sample was then transferred to another three-chamber HWCVD for growing the

intrinsic and p-type layer of the structure [20]. Thin 20 nm nucleation layer was grown at 400°C substrate temperature with filament temperature 1900°C along a gas ratio of SiH_4:H_2 = 1:20 for 100 sec. In order to grow thick silicon film, a mixture of SiH_4 and H_2 were used as process gas with a ratio of SiH_4:H_2=5:15 for 20 min [21], [22]. A thin 5 nm layer of amorphous intrinsic poly silicon film was grown at this 200°C for 15 sec using a gas ratio of SiH_4:H_2=1:20. This layer acts as a passivating interface layer between the polycrystalline silicon and amorphous silicon emitter. The thickness of the layers are estimated from the cross section transmission electron microscopy [23]. Amorphous p-type silicon film was grown on top of amorphous intrinsic thin silicon layer. Amorphous boron doped p-type 10 nm thin silicon layer was grown at 200°C substrate temperature with filament temperature 1900°C for 50 sec [24]. Thermal evaporator and chemical etching was used to make front and back contact respectively. Stainless steel mask with 1mm diameter hole separated by 3 mm was used to deposit 100nm aluminium in a thermal evaporator for 18 top contacts. To reach the back contact, deposited silicon was removed from near the edge. 30 ml of Tetra methyl ammonium hydroxide (TMAH) was heated at 90°C for 15 minutes in a petri dish. Using a suitable clamp, the sample was dipped 2 mm into the solution for 2 minutes to etch one micron of silicon film form the edge.

A schematic of the n-i-p structure fabricated in this work is shown in Figs. 1 and 2. Table 1 shows detail of the growth parameters used for fabricating the structure.

Table 1. Growth parameter of n-i-p hetero junction diode fabrication process using HWCVD on FTO coated glass substrate (Sample 99_n-i-p_dev, 100_n-i-p_dev)

Step	Process gas pressure mbar	Substrate heater temp. °C	Filament temp. °C	Gas flow ratio sccm	Duration	Thickness nm	Growth Rate A°/Sec
1	6.6×10^{-2}	350	1650	SiH_4:PH_3:H_2=2:1:50	32 min	180	1
2	6.7×10^{-2}	400	1896	SiH_4:H_2=1:20	100 sec	20	2
3	7.3×10^{-2}	700	1886	SiH_4:H_2=1.5:20	100 sec		__
4	6.4×10^{-2}	700	1906	SiH_4:H_2=2:18	100 sec	214	7
5	6.7×10^{-2}	700	1908	SiH_4:H_2=3:17	100 sec		__
6	7.1×10^{-2}	700	1906	SiH_4:H_2=5:15	20 min	805	7
7	5.5×10^{-2}	600	1898	H_2=20	30 min	Passivation	__
8	5.6×10^{-2}	600 to 200	1892	H_2=20	50 min	Cooling	__
9	6.7×10^{-2}	200	1886	SiH_4:H_2=1:20	15 sec	5	2
10	1.2×10^{-2}	200	1868	SiH_4:B_2H_6:H_2=1:2.2:20	50 sec	10	2

3. Result and discussion

We have deposited the n-type silicon on FTO coated glass as collector. The intrinsic polycrystalline silicon layer is used as the base absorber. Absorption of high energy photon and resulting electron hole pair generation occurs in the absorber layer. The intrinsic thin layer acts as a passivation layer in a hetero junction to reduce the defect density at the interface with the absorber layer (which reduces the interface recombination) while admitting a maximum amount of light to the absorber layer.

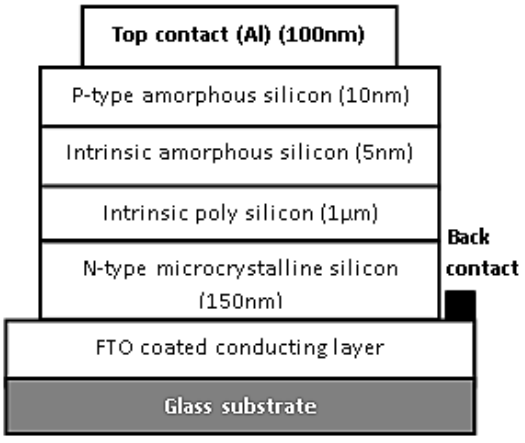

Fig. 1. 2D block diagram of HIT structured n-i-p diode

Well passivated absorber layer also prevents recombination of charge carrier before reaching the contacts, improving the device performance [25].

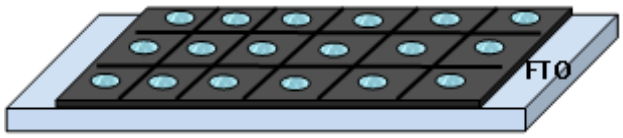

Fig. 2. Schematic of n-i-p diode on FTO coated glass (color online)

3.1. Current-voltage characteristics

The dark I-V curves for two devices are shown in Figs. 3 and 4. Both the devices shows diode behaviour [26]. The contacts were made between one dot from the top and the back FTO. The rectification ratio from the current flow for applied voltage of 0.8 V in the forward bias direction and -0.8 V in the reverse bias direction is about 15 for 99_Dev_10 shown in Fig. 3 and 25 for 100_Dev_C3 shown in Fig. 4 [27]. From the dark forward bias I-V characteristics, the series resistance is, as estimated using Norde's method [28] from applied forward voltage between 0.8 V to 1V about $8\times10^4\Omega$ for sample 99_Dev and $1.5\times10^4\Omega$ for 100_Dev [29], [30].

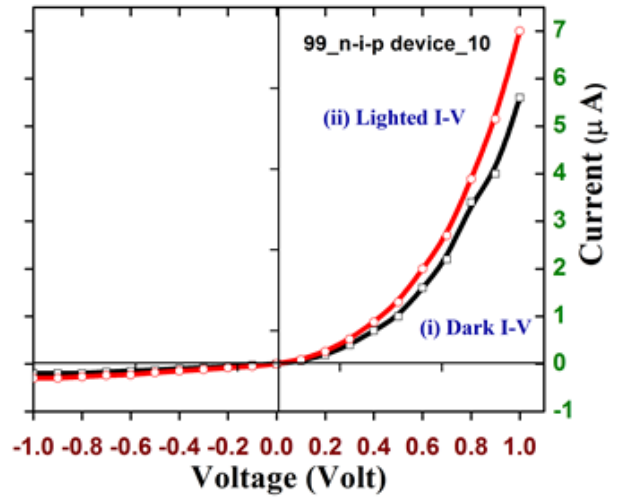

Fig. 3. Dark and lighted current-voltage (I-V) curve of 99_Dev n-i-p diode with circular top contact (color online)

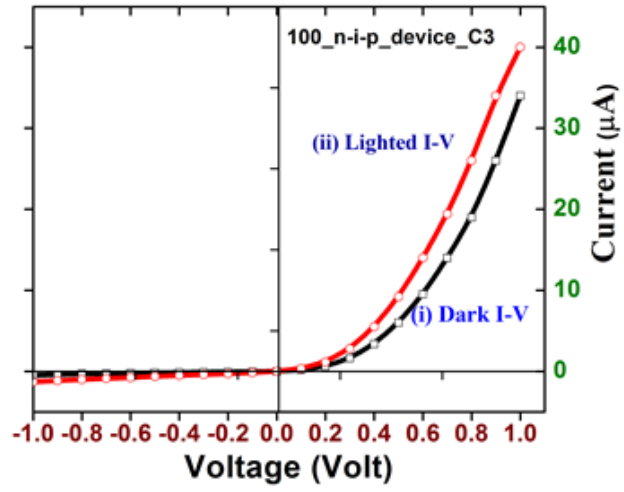

Fig. 4. Dark and lighted current-voltage (I-V) curve of 100_n-i-p diode with circular top contact (color online)

It is clear that the dark current is not dominated by injection of charge carriers across the junction, but by a resistive region. It is possible that the resistive region has lot of defects so that the injected minority carriers are able to modify the conduction to only a small extent. The effect of shining a white light (~50mW/cm^2) is seen as only a small enhancement of current above the dark current similar as a photoconductor. Possibilities for the absence of photo voltage are, i) doping in the n+ and p+ regions is not sufficiently high to deplete the absorber layer completely and ii) the region near the junction between the intrinsic silicon layer and a-Si:H / p-type a-Si:H layer is of poor quality. This region, which is supposed to separate the photo-generated excess electrons and holes to develop the photo voltage, instead it allows recombination of carriers such that no separation of electrons and holes occurs. The small enhancement of current under light is likely due to reduction in the resistance of the intrinsic silicon film. To understand this aspect better, Capacitance-Voltage (C-V) measurements were carried out on the devices, as described in the next section.

3.2. Capacitance-voltage characteristics

We have measured capacitance for various bias voltage using Agilent 4284A precision inductance, capacitance, resistance (LRC) meter. The capacitance is measured by superimposing a small ac voltage of frequency 555 Hz on the dc bias voltage. Results of these measurement are plotted as C-V graph and $1/C^2$ –V graph as shown in figure 5. The estimated depletion width at 0 bias is about 850 nm with 1mm diameter top contacts on sample 99_dev as given in Table 2 [31]. The depletion width is comparable to the thickness of the grown film.

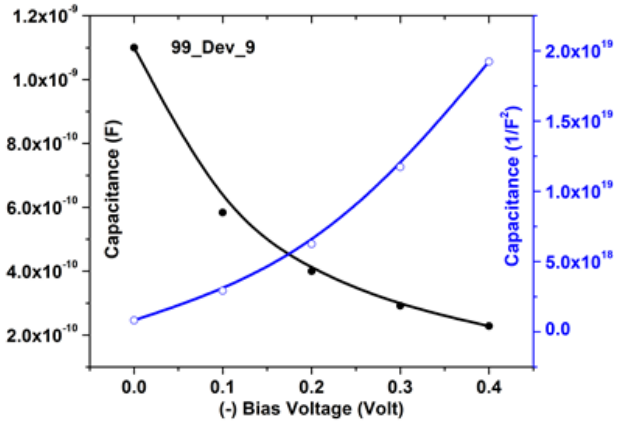

Fig. 5. Capacitance-voltage (C-V) curve of 99_Dev_9 n-i-p diode with circular top contact (color online)

Ideally, it would require n+ and p+ layers are to be sufficiently doped to fully deplete the thickness of the undoped i-layer at zero bias and even at some forward bias. This would ensure that the intrinsic layer is having electric field to separate the photo generated carriers. As such, the diffusion length of excess carriers in the intrinsic layer is expected to be negligible so that separation of charge carriers will depend entirely on the electric field,

which requires full depletion of the intrinsic region. Since photoconductivity was seen, it is anticipated that an increase in the doping concentration of n+ and p+ regions, and adjusting the thickness of the intrinsic layer so that it is fully depleted at zero bias and even at some forward bias, the device may exhibit photo-voltage. The $1/C^2$ - V curve is not a straight line. It is not expected to be linear since there will be deep level traps which change their filling with application of bias. The resulting charge concentration in the depletion region will not be constant as required for straight line behaviour. Therefore, the concentration values shown Table-2 are only suggestive of the concentration in the intrinsic region.

Table 2. Estimation of depletion width and majority carrier concentration from capacitance measurement for n-i-p diode

Sample name	**Capacitance at zero bias (F)**	**Device area (cm^2)**	**Depletion width (nm)**	**Slope of $1/C^2$ –V curve (F^{-2}-V^{-1})**	**Majority carrier concentration (atom-cm^{-3})**
99_Dev_9	4.35×10^{-10}	0.09	850	2.3×10^{19}	2×10^{13}

4. Conclusion

We have described the fabrication of n-i-p structured hetero-junction device synthesized by HWCVD on glass substrate. The dark I-V of the single top contact showed diode characteristics and with white light, small photoconductivity was observed. Photovoltage was not observed because of insufficient depletion of the undoped absorber layer. Analysis shows that improvement in the doping of n+ and p+ regions is necessary. For optoelectronic application, further optimization of the proposed composite structure including the quality of the film and interfaces would be necessary. This could involve depositing all the layers in a single HWCVD system.

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