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Influence of thermal annealing on the memory effect in MIS structures containing crystalline Si nanoparticles

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Silicon nanocrystals embedded in a SiO_2 matrix are fabricated by thermal annealing of Metal/SiO_2/SiO_x/c-Si structures (x=1.15) at 1000 ^oC in N_2 atmosphere for 30 or 60 min. High frequency C-V measurements demonstrate that both types of sample can be charged negatively or positively by applying a positive or negative bias voltage to the gate. The clockwise hysteresis windows of 30 and 60 min annealed samples are about 7 and 5.5 V for the ± 12 V scanning range (E_{ox} = ± 2.4 MV/cm), respectively. Although the samples annealed for 60 min have a smaller hysteresis window, they have two important advantages compared to the 30 min annealed ones: a lower defect density at the c-Si wafer/SiO_2 interface and a smaller value of the fixed oxide charge close to this interface.

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1. Introduction

Metal-Insulator-Silicon (MIS) structures with an insulating layer containing silicon nanocrystals (NC) are being actively studied [1-3] since they are promising for application in distributed floating gate memory devices [4]. The usage of nanocrystals as discrete charge storage nodes can result in better stability compared to the conventional floating gate memory device. The extremely small thickness of the dielectric layer between the crystalline silicon wafer and the nanocrystals leads to low operation voltages and shorter write/erase times. MIS structures with NCs allow an extension of the scaling and thus increasing the information density.

Various methods have been used to fabricate MIS structures containing silicon NCs in a dielectric matrix: ion implantation of Si^+ ions in silicon dioxide [2,5], chemical vapour deposition of silicon, followed by thermal oxidation [1,6], thermal evaporation [3] etc.

In order to make use of the advantages of the NC based memories, optimization of the technological processes in regard to the size and density of the NCs, properties of the c-Si wafer/insulator interface, density of traps in the multilayer dielectric and properties of the interface nanocrystal/dielectric matrix is necessary.

In this work, we present results about the influence of the annealing time on the charging effects of Si nanocrystals, which are formed by high temperature annealing of SiO_x layers prepared by physical vapour deposition in an inert gas ambient.

2. Experimental details

The experimental structures used in this study were fabricated by thermal evaporation of a SiO_x (x=1.15) layer [7] with a thickness of about 15 nm on top of n-type crystalline silicon with a resistivity of 4-6 Ω cm, followed by radio frequency sputtering of a silicon dioxide layer of thickness ~ 40 nm. Before the SiO_x layer deposition, the silicon wafer was cleaned chemically by a standard (for the microelectronics industry) procedure. In order to grow crystalline silicon (c-Si) nanoparticles, the structures were annealed at 1000^{o}C in a N_2 atmosphere for 30 or 60 min [7,8]. The annealing process was used not only for phase separation, growing of silicon nanocrystals and transformation of the SiO_x into SiO_2 [7], but also for formation of a silicon dioxide layer between the nanocrystals and substrate that has a tunneling thickness. After the annealing procedure. Al metallization was carried out through a mask and capacitors with area of 2×10^{-3} cm^{-2} were formed. Aluminium was also used as a back contact to the crystalline silicon. Fig. 1 shows schematically a cross-section of the experimental structures.

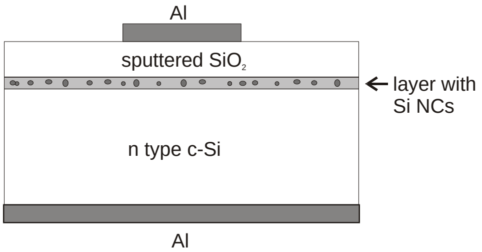

Fig. 1. Schematic cross-section of the experimental structures.

The memory effect was studied by high frequency capacitance-voltage (C-V) measurements at 100 kHz in the dark at room temperature. In the measurements, all gate biases were taken relative to the back contact. Stokes Raman spectra were measured using a 532 nm laser line. In order to avoid the strong Raman scattering from the c-Si substrate, the measurements were performed on identically prepared layers deposited on quartz substrates. HREM measurements were performed on SiO_x films deposited on Si substrates and annealed at 1000 °C by means of a JEM 4000 EX electron microscope operating at 400 kV. Electron micrographs were recorded at 500 000 times magnification using optimum contrast conditions ~ near Scherzer defocus.

3. Results and discussion

Fig. 2 shows a cross-section micrograph of the SiO_2 layer with silicon NCs. It is seen that the nanocrystals are uniformly distributed in the dielectric matrix. The average size of the Si NCs is 4.3 nm, and the filling factor is about 5 volume %.

The Raman scattering spectrum of a SiO_x film with initial x=1.15 annealed at 1000 °C for 60 min is depicted in Fig. 3 along with the spectrum of a non-annealed reference sample. An asymmetric band is well seen in the spectrum of the annealed SiO_x film, which is peaked at 516 cm^{-1}. It is red-shifted with respect to the band from c-Si (521 cm^{-1}) and indicates the presence of nano-sized crystalline Si, thus proving the formation of Si nanocrystals upon annealing.

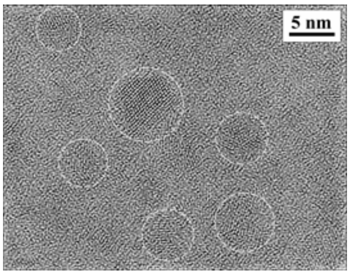

Fig. 2. Cross-section of the SiO_2 layer with silicon nanocrystals.

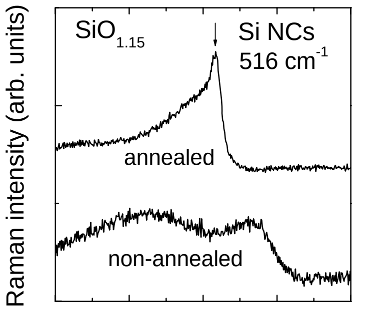

Fig. 3. Raman scattering spectra of a SiO_x film on a quartz substrate with initial x=1.15, annealed at 1000 °C for 60 min and a non-annealed reference sample.

In Fig. 4, the high frequency C-V hysteresis dependencies of an as-deposited non-annealed sample are shown. The C-V curves are normalized to the capacitance in accumulation, ~ 135 pF. From the capacitance in accumulation, an effective thickness of the dielectric layer has been calculated having a value of about 50 nm. Curve 1 was measured in the range (0 - 1.5V) and back, while curves 2 and 3 were measured in the ranges ± 5 V and ± 8 V, respectively. In all scans, the gate bias was first swept from positive to negative voltage and then in the reverse direction. From the position of the initial C-V characteristic (curve 1), it is clear that even at +5 (-5 V) the structure goes into a deep accumulation (inversion) condition.

One can see from Fig. 4 that a negative gate bias (-5 or -8 V) shifts the C-V curve towards more negative voltages, but positive biases (+5 or +8 V) do not shift the curve to more positive voltages compared to the initial one (curve 1). Moreover, the application of a higher positive bias causes a shift which corresponds to a smaller value of the trapped negative charge (see the right branches of curves 3 and 2). Furthermore, the slope of the C-V curve depends on the sign of the charging bias (compare the left parts of curves 2 and 3 measured after charging the structure with negative bias with their right parts measured after charging the structure with positive bias). The variation of the curve's slope indicates that charge is trapped at or close to the interface c-Si wafer/dielectric layer. Another feature of the as-deposited structures is that they lose the charge created by negative bias too fast (for several min). Hence, although some hysteresis is observed in the as-deposited sample, it is not suitable for memory device application.

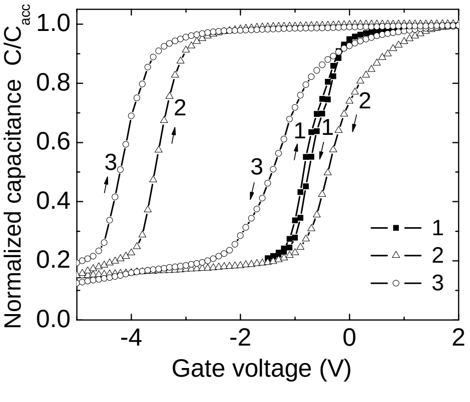

Fig. 4. Normalized high frequency C-V curves of an as-deposited sample measured at 100 kHz: curve 1 – measured by sweeping the gate voltage between 0 and -1.5 V and back, curves 2 and 3 - by sweeping in the ranges ± 5 V and ± 8 V, respectively. The voltage sweep rate was 0.2 V/s.

Fig. 5 a, b show the normalized C-V hysteresis curves of samples annealed at 1000 °C for 30 and 60 min, respectively, measured in the ranges ± 12 V and ± 15 V. The observed clockwise hysteresis for both types of structure can be explained by assuming charging of the

nanocrystals with electrons/holes, which tunnel from the substrate through the thin oxide at positive/negative biases. The value of the hysteresis is about 7 and 12 V (a) and 5.5 and 10.5 V (b) for ± 12 V and ± 15 V scanning ranges.
One essential difference between the C-V curves of both types of sample is that the curves in Fig. 5b (60 min annealed sample) are shifted in parallel, while the slope of those in Fig. 5a depends on the sign of the charging bias. Additionally, the lefthand parts of curves 2 and 3 in Fig. 5a are much steeper than the righthand parts (and have approximately the same slope as the curves in Fig. 5b). These observations indicate that after a 30 min annealing the sample still has a high density of interface defects. Therefore the larger hysteresis value of the 30 min annealed sample may contain a significant contribution of defects at the c-Si wafer/SiO_2 interface. An advantage of the sample annealed for 60 minutes is also the smaller value of the flat-band voltage V_{FB} of the initial curve, which means a smaller density of the fixed oxide charge. V_{FB} is the voltage corresponding to the flat-band capacitance of the structure C_{FBS}, and for calculation of C_{FBS} the standard expression [9] has been used. The V_{FB} of curve 1 in Fig. 5b is ~ -3.9 V, while in Fig. 5a it is ~ -6.6 V. This also implies a better quality of the interfacial region in the case of 60 min annealing time.

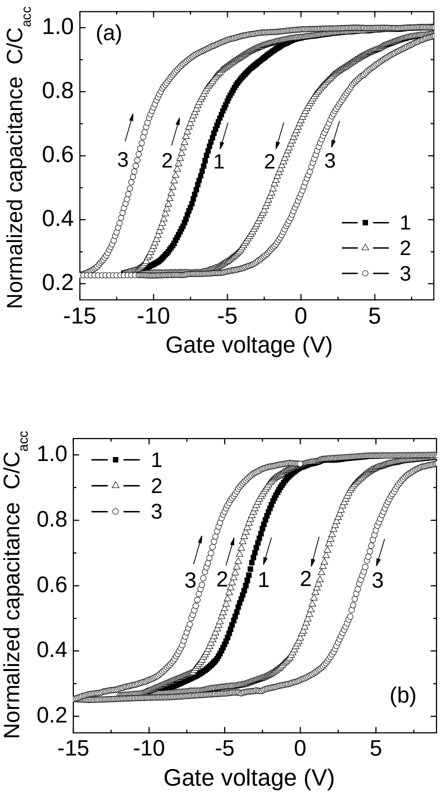

Fig. 5. Normalized high frequency C-V hysteresis curves measured at 100 kHz for samples annealed at 1000 °C for 30 min (a) and 60 min (b). The scan ranges are ± 12 V (curve 2) and ± 15 V (curve 3). The initially measured curve is denoted as curve 1. The voltage sweep rate was 0.2 V/s.

In Fig. 6, the retention characteristics of both types of sample after charging with +12 or -12 V are shown. The value of the flat-band voltage has been measured during a time interval of about 24 h and used to obtain the flat-band voltage shifts ΔV_{FB}. It is seen that the charge loss approximately follows an exponential law. Two regions with different decay constants can be distinguished in the characteristic of the 30 min annealed sample, with faster discharge during the first few hours. One may speculate that in this time interval the carriers captured at/or close to the c-Si wafer/SiO_2 interface succeed in escaping from the traps and return back to the c-Si due to the internal electric field. Both types of sample lose about 50 % of the trapped charge after 24 h when charged with a positive voltage.

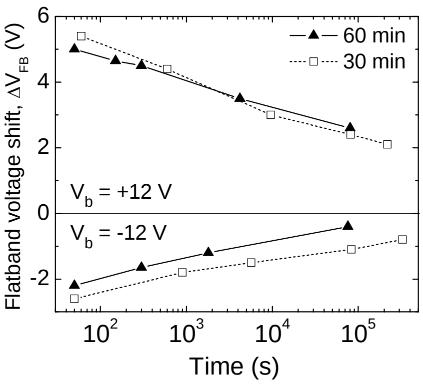

Fig. 6. Charge retention characteristics of samples annealed at 1000 °C for 60 min (solid symbols) or 30 min (open symbols) after charging the nanocrystals with V_b of +12 or -12 V.

4. Conclusion

Silicon nanocrystals embedded in a SiO_2 matrix were fabricated by thermal annealing of SiO_2/SiO_x/c-Si structures at 1000 °C in a N_2 atmosphere for 30 or 60 min. The high frequency C-V curves of the 30 and 60 min annealed samples have hysteresis windows of about 7 and 5.5 V for a ± 12 V scanning range (E_{ox} = ± 2.4 MV/cm), respectively. The structures annealed for 60 min have a better interface with the c-Si wafer than the ones annealed for 30 min, i.e. a lower defect density at the c-Si wafer/SiO_2 interface and a smaller value of the fixed oxide charge close to it. Both types of sample lose about 50% of the trapped charge after 24 h, when charged negatively. Further optimization of the structures in regard to improving the quality of the tunnel oxide and thus the retention characteristics is necessary.

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