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Investigations of AlSb thin films grown on Si by liquid phase epitaxy

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Heterojunctions devices of n-AlSb/p-Si were fabricated by growing n-AlSb films onto p-type Si single crystal waferes using liquid phase epitaxy (LPE) . The X-ray diffraction studies indicate that all films were monocrystalline with single AlSb phase and showing one significant peak oriented along the (111) direction with cubic structure. Current – voltage (I-V) and capacitance – voltage (C-V) measurements were performed to determine the electrical characteristics of these structures. Rectifying properties were obtained, which are definitely of the diode type . The analysis of the dark I-V characteristics of n-AlSb/p-Si at several temperatures with respect to the elucidation of conduction mechanisms and evaluation of the heterojunction parameters is presented . The forward current increases exponentially with the applied voltage at low voltaje region ,which was dominated by the thermionic emission over the n-AlSb/p-Si whereas at high voltage region the process is dominated by the series resistance . The carrier transport mechanism was considered to be mainly generation and recombination of carriers in the p-Si substrate under the reverse bias . Information on the and the built – in potential and other important junction parameters can be sucsesfully obtained by studying the dark C-V measurements at 1 MHz . Discussion of the obtained results and their comparison with the previous published data are also given.

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1.Introduction

Antimonide-based compounds offer a wide variety of electronic band gaps from 0.17 to 1.58 eV, band gap offsets, and electronic barriers along with extremely high electron mobility, therefore, enable a variety of high-speed and low-power consumption electronic devices than equivalent InP- and GaAs-based devices [1] and infrared light sources [2,3]. Epitaxial growth of Sb-based compounds on GaAs and Si substrate is very interesting since it has several advantages, including its high quality with semi-insulating, large area, and low cost compared with substrates of GaSb and InAs. In addition it affords the possibility of integration for optoelectronics device, such as laser diode [4], detectors [5], and transistor [6]. Therefore, much effort has been devoted to growing high-quality Sbbased layer on GaAs and Si substrates. However, in spite of advantage of performances, there is fundamental problem in the growth of III-Sb-based compound semiconductors on GaAs and Si substrate.

AlSb was originally a material system of great interest because of its potential applications in electronic and photonic devices at high temperatures such as transistors, p–n junction diodes [7] and photovoltaic cells [8].

The molecular beam epitaxy (MBE),the metal – organic chemical vapor deposition (MOCVD) and their new modern modifications such as chemical beam epitaxy (CBE) , atomic layer epitaxy (ALE) and so on had proved the possibility to prepare epitaxial films [9] .

Nevertheless, the liquid phase growth methods are still useful for those devices. With their structural perfection and their purity the liquid phase epitaxy (LPE) [10] layers are not inferior to the layers, grown by the above mentioned gas phase epitaxy methods. The single crystals growth is always carried out from a liquid phase. All above means that the investigation of the processes, occurring in the phase boundary region between the liquid phase and the solid phase, is very important for obtaining a high quality of the grown AlSb on Si. As a result, we which exhibit structural coherence and reasonably good electrical properties.

As mentioned above, the study of semiconductor heterojunctions have been a topic of great interest due to their wide spread use in numerous optical and electronic devices. Therefore, we have extended our studies of heterojunction preparation using LPE and investigate the dependence of the current-voltage characteristics on the temperature in both forward and reverse bias in an attempt to obtain information on the transport mechanisms of n-AlSb/p-Si devices. In addition, the capacitance–voltage measurements were applied for characterization of these heterojunctions .

2. Experimental details

The liquid phase epitaxy technique was employed to grow layers of n-AlSb on p-Si substrate single crystal wafers using indium as a solvent. The multibin boat made of special graphite hardness is held in a fixed position

within a silica tube , and a thermocouple is fixed under the boat . Prior to the growth run , purified argon is passed through the tube . The technique of LPE is described in detail elswhere [11,12]. The loaded boat was heated up to 350 K and kept at this temperature for 30 min to homogenize the solution and then cooled down to 280 K with a cooling rate of 10 K/min . The growth process is terminated by removing the ready substrate with its upper layer from the solution cell . The surface of the obtained layers was examined by the SEM model JEOL JXA-840 A.

In order to measure the electrical properties of the devices, electrical contacts were equipped with copper wires mechanically applied to the two metal electrodes using thermosetting silver paint. The current flowing through the sample was determined using a stabilized power supply and a high-impedance Keithley 617 electrometer . Electrical properties were performed in dark over the temperature range 293-373 K . The temperature was measured directly by means of chromel-alumel thermocouple connected to hand - held digital thermometer (Extech 421508). Capacitance-voltage measurements were performed at 1MHz , using a computerized capacitance- voltage system consisting of the 410 C-V meter interfaced via model 4108 C-V interface .

3. Results and discussion

3.1 Structural characteristics

The surface topography of the epilayer of AlSb grown on p-Si single crystal by LPE was examined by SEM . It is clear from the SEM micrograph , shown in Fig.1, that fine crystallites are epitaxially grown which may correspond to the n-AlSb epilayer .

Fig.1 Scanning electron micrograph of AlSb films on p-Si substrate.

Fig.2 shows the X-ray diffraction patterns of the grown n-AlSb film on p-Si single crystal .

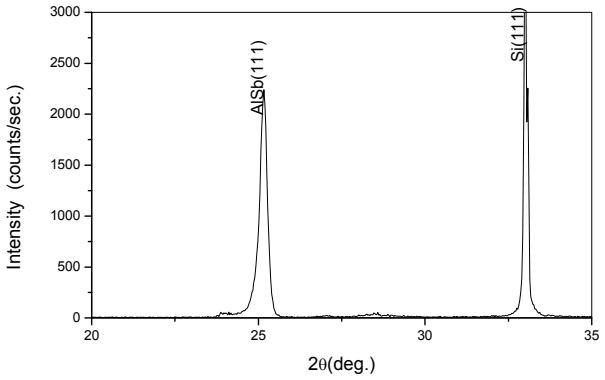

Fig.2 XRD of n-AlSb/p-Si heterojunction.

It is worth mentioning that the X-ray diffraction chart shows two discrete sharp peaks confirming the monocrystalline structure of both AlSb and Si with the same (111) orientation . The comparatively higher peak intensity oriented confirms the monocrystalline cubic structure of the Si substrate while the other peak belongs to the monocrystalline cubic AlSb epilayer (according to JCPDS card no.75-0446) with interplanar spacing value of 3.53 A . It is clearly confirmed that the direct LPE growth yields a monocrystalline AlSb film on p-Si wafer because of the nearly lattice match between them. This result is considered as an attempt to improve the quality of the grown films by LPE for several electro-optic and electronic device applications [13].

3.2. Current - Voltage characteristics

The current-voltage characteristics of the AlSb/p-Si heterojunction at room temperature (298 K) in the dark is shown in Fig.3 .

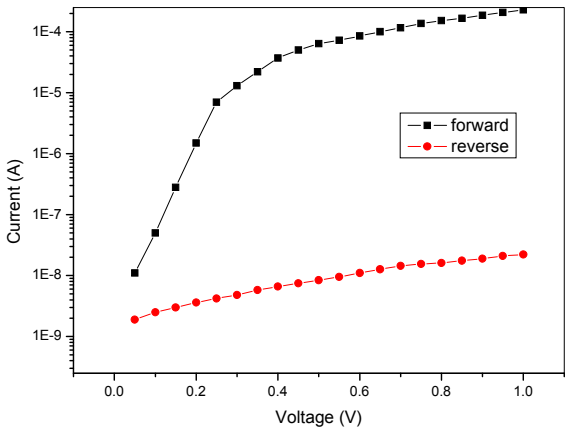

Fig. 3. Semi-logarithmic plot of both forward and reverse current versus applied voltage at room temperatures (298 K).

As observed the characteristic was definitely of the diode type, with he forward direction corresponding to the negative potential on AlSb. This behaviour can be understood with interface to a n-p junction, namely the barrier at the interface limits the forward and reverse carrier flows across the junction, where the built-in potential could be developed . Thus the device clearly exhibits good rectifying characteristics . The rectification ratio , RR , is calculated as the ratio of the forward current to the reverse current at a certain applied voltage . The obtained values of the rectification ratio RR are determined at different temperatures and listed in Table 1 .

Table 1. Temperature dependence values of various parameters determined from I-V characteristics of AlSb/p-Si heterojunction.

T(K)	I_0(A)	**Φ**(eV)	n	R_s(kΩ)	RR
298	$2x10^{-9}$	0.78	1.19	2.7	5600
323	$7.3x10^{-7}$	0.81	1.2	0.662	4100
348	$1.2x10^{-7}$	0.8	1.27	0.41	890
373	$3.6x10^{-7}$	0.82	1.295	0.33	500

It is obvious that RR at room temperature (298 K) has the best rectification, indicating the good performance of the device at room temperature.

The semilog-forward bias I-V characteristics of AlSb/p-Si heterojunction are shown in the temperature range of 298-373 K in Fig. 4.

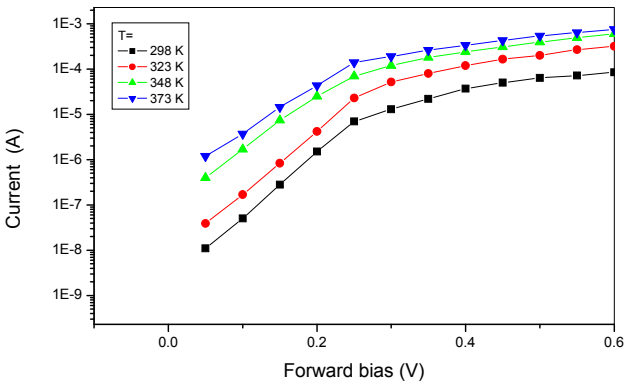

Fig.4 Semi-logarithmic plot of forward current againt applied voltage at different temperatures.

As observed, the forward bias I-V characteristics are linear over the entire temperature range at low forward bias voltage but deviate considerably from linearity due to the effect of some factors at large voltage. The downward concave curvature of the forward bias I-V plots at sufficiently large voltage (V > 0.3 V) has been attributed to the effect of series resistance R_s from contact wires or bulk resistance of the semiconductor, the interfacial layer, and the interface states. The series resistance, R_s, is significant in the downward curvature of the forward bias I-V characteristics, but the other two parameters are significant in both the linear and non-linear regions of the I-V characteristics .

At large forward voltages, the horizontal displacement different ΔV gives the voltage drop IR_s across the neutral region. By plotting ΔV against I (Fig. 5), the value of R_s was calculated to be in the order of 2700 Ω at room temperature.

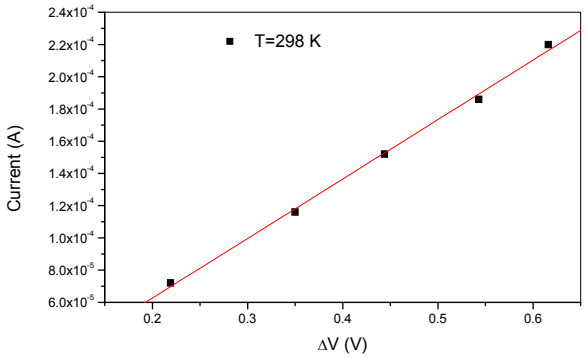

Fig. 5 The voltage drop across the series resistance versus I.

The R_s values are determined in the temperature range 298-373 K and listed in Table (1). As shown. The ncrease of series resistance with the decrease in temperature may be attributed to the lack of free carrier concentration at low temperature.

It can be assumed that the current-voltage characteristics are described by relation which takes into account the thermionic emission at AlSb-Si contact barrier, where a modification for a series resistance must be introduced at higher current.

Therefore, the current is related to the voltage by the equations [15]

$$I = I_0\left[\exp\left(\frac{qV}{nKT}\right)-1\right] \quad \text{at low current densities} \quad (1)$$

$$I = I_0\left[\exp\left(\frac{q(V-IR_s)}{nkT}\right)-1\right] \quad \text{at higher current densities} \quad (2)$$

where q is the electronic charge , n the ideality factor, k the Boltzmann constant , R_s the series resistance and I_0 the saturation current at zero voltage , is given by

$$I_0 = AA^* \exp\left(\frac{-q\Phi}{kT}\right) \quad (3)$$

where A is the junction area , A* (A* =4π q m*k^2/h^3) the effective Richardson constant , m* is the effective mass of carriers and Φ the barrier height of the contact barrier . Generally , barrier height,Φ , is determined from ln I versus V plots (Fig. 4) . For voltages larger than kT/q, this plot would be a straight line whose extrapolated intercept with zero voltage axis would give I_0 which could be used to derive Φ by using Eq. (3) . The values of the saturation current I_0 and barrier height Φ at different temperatures, ranging from 298 to 373 K , are obtained and listed in Table 1.

The inverse slope of the linear region of the forward bias ln I -V characteristics in Fig.4 can be used to determine the ideality factor along Eq.(4) :

$$n = \frac{q}{kT}\frac{dV}{d(\ln I)} \quad (4)$$

The ideality factor of the AlSb/p-Si heterojunctions at different temperatures are also obtained and listed in Table 1 .The slight deviation of the diode ideality factor from unity may be attributed to the different quality of the semiconductor surfaces, which is in agreement with the common experience that in most practical semiconductor junctions the ideal situation is seldom realized. This indicates that the I-V plots exhibit departures from the ideal thermionic emission, TE, behavior. The best value of the ideality factor is obtained at room temperature (298 K).

The temperature dependence of the barrier height Φ and ideality factor n is shown in Fig. 6.

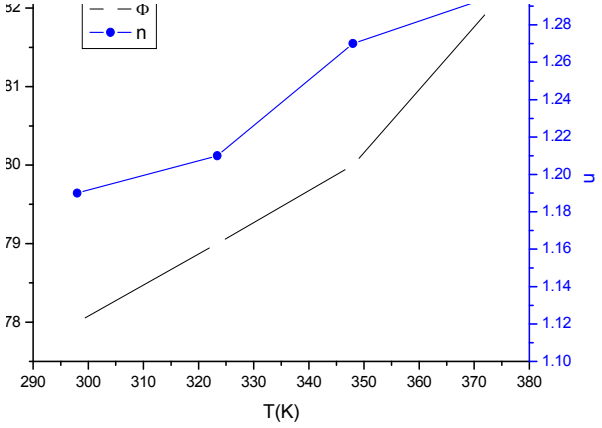

Fig..6 The temperature dependence of the barrier height and ideality factor.

As observed from Fig.6, the increase in the barrier height Φ and the increase of the ideality factor n as the temperature increased can be attributed to the effect of carrier generation –recombination [14] .

The dark current I_R is plotted against the reverse voltage in Fig.7 ; this shows a slow linear increase of the current with voltage , not predicted for a pure thermionic emission , as given by Eq.(3) .

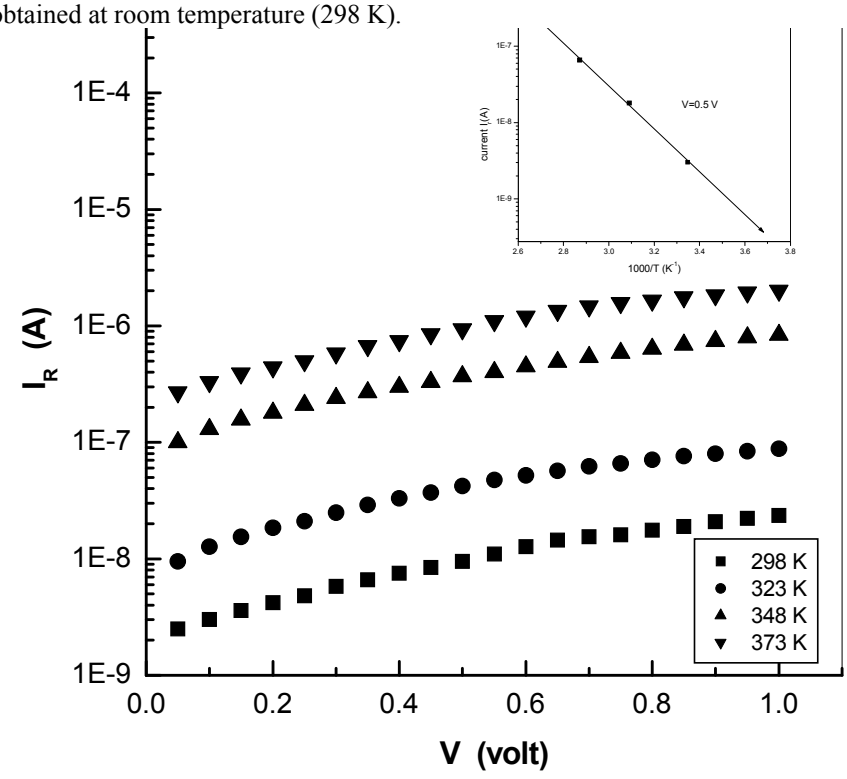

Fig.7. Reverse-current voltage characteristics at different temperatures . The inset shows semi-logarithmic plots of reverse current versus 1/T at higher voltage bias.

There are several reasons why the reverse current does not saturate at the value of I_0 . One possibility is that the barrier height is dependent on the electric field strength inside the barrier itself. Since the maximum field strength in the barrier, E_{max}, increases with the reverse bias , it follows that the barrier height decreases by increasing the reverse voltage ;consequently , the current does not saturate but increases proportionally with $\exp(q\Delta\Phi/kT)$, where $\Delta\Phi$ is the reduction of the barrier height due to the field variation. However, as reported later , it has been found that the capacitance-voltage characteristics , under reverse bias are very consistent with a capacitance model in the absence of surface states, where the barrier height is independent of voltage.

Another reason can be the effect of tunneling. A reverse bias of a few volts can decrease the barrier thickness enough for tunneling to take place. In this case, the current is still an exponential function of the forward voltage. A third possibility is that generation and recombination of charges in the bulk of the Si substrate are the dominant processes determining the reverse current. In this latter case the dark current density is given by [15]

$$I_R \alpha \exp\left(\frac{E_g}{rkT}\right) \tag{5}$$

where r = 2 for generation and recombination process occurring via mid band gap states. Thus, if the main source of the reverse current is due to the carrier generation on the Si rather than carriers originating in the AlSb/Si interface or in the AlSb layer , it is expected to be thermally activated with energy $\Delta E = E_g/2 \simeq 0.55$ eV (where $E_{gSi} \simeq 1.12$ eV). Thus a semilogarithmic plot of the reverse current against $^1/_T$ is shown in the inset of Fig.7 . A reasonably good fit was obtained and gives the fitted value of $\Delta E \simeq 0.57$ eV. This energy is approximately one half of the band gap of n-Si, which suggests that the dark reverse current does indeed originate in the p-Si.

The barrier height Φ was also calculated from measurements of the capacitance as a function of voltage.

The capacitance under reverse bias V_R is given by [15]

$$C = \left(\frac{qNA^2\varepsilon_s}{2}\right)^{1/2}\left(\Phi - \zeta + V_R - \frac{kT}{q}\right)^{-1/2} \tag{6}$$

where

ε_s is the permittivity of the inorganic semiconductor, N the carrier concentration and ζ the depth of the Fermi level below the conduction band. If the barrier height is independent of the reverse bias, i.e. there is no appreciable interfacial layer, a plot of C^{-2} against V_R should give a straight line with intercept $-V_i$ (built-in potential) on the horizontal axis equal to $-(\Phi - \zeta - \frac{kT}{q})$. The barrier height is then given by

$$\Phi = V_i + \zeta + \frac{kT}{q} \tag{7}$$

In this case, the carrier concentration can be determined from the slope of the plot C^{-2} versus V_R by the relation

$$\frac{d(C^{-2})}{dV_R} = \frac{2}{q\varepsilon_s NA^2} \tag{8}$$

The distance ζ of the Fermi energy below the conduction band, and hence the barrier height Φ , can be obtained by finding N from Eq. (8), since

$$\zeta = \frac{kT}{q}\ln\left(\frac{N_c}{N}\right) \tag{9}$$

where N_c is the effective density of states in the conduction band . A plot of C^{-2} against V_R is shown in Fig. 8, where a value of 86 mV for the intercept on the x-axis (Vi) can be obtained. From the slope of the plot shown in Fig. 8 and by using 11.7 as the dielectric constant of Si , a value of $4.5\text{x}10^{15}$ cm^{-3} for N was calculated.

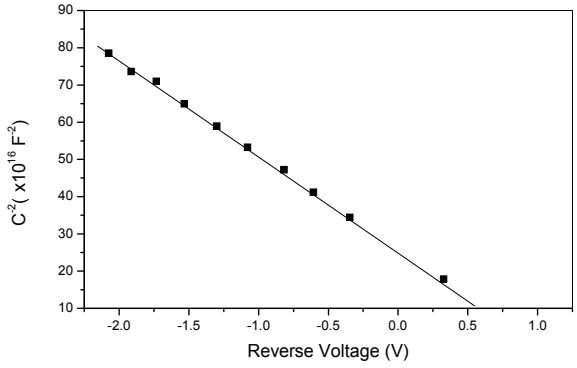

Fig. 8.C-V characteristics of the Al Sb/p-Si heterojunction at 1MHz

This value of N, which agrees perfectly with the resistivity of the p-doped silicon used in this work, was obtained by considering the contact surface between the silicon and AlSb as the active junction area; in contrast, when the surface of the metallic contacts was taken as the junction area, an unrealistic value for the charge density of silicon was found. By using the above value of N and 3

X 10^{19} cm^{-3} as the effective charge density of Si (N_c), the depth ζ of the Fermi level was found to be 0.23 eV. By substituting the numerical values in Eq, (7), a barrier height Φ of 0.79 eV was obtained. It can be shown that the values of the barrier height obtained at room temperature (298 K) using *I-V* and C-V methods are similar. This probably means that the high value obtained for *n* is not due to a high density of interface states.

4. Conclusions

From the present work we concluded that:

X-ray diffraction analysis confirmed a well grown monocrystalline n-AlSb epilayer on p- Si single crystal substrate.

These junctions exhibit rectifying characteristics indicating a p-n diode – like behavior. The dark current – voltage measurements suggest that the forward current transport in these junctions involve thermionic emission of the electrons from p-Si over the AlSb/Si barrier at low forward bias. At higher voltages , the trend is no longer exponential swing to a series resistance inherent in the neutral region of the semiconductor . On the other hand, the reverse current can be explained by the generation – recombination of carriers in the p-Si substrate.

From the capacitance – voltage measurements at high frequency (1MHz), one can obtain information about the depletion layer extending in the Si side regardless the AlSb side. These characteristics are reasonably interpreted by assuming the abrupt heterojunction model.

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