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Laser processed hydrogenated amorphous silicon for field emission displays♣

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Amorphous silicon is now considered to be a mature technology in the field of flat panel displays. The a-Si:H Thin Film Transistor has enabled the active matrix liquid crystal display that has become the standard. However, the technology is still not perfect and suffers from visual artefacts, especially when trying to render video rate images. Field emission displays (FED) have promised to resolve these issues, but lithographic limitations in the technology have so far failed to deliver a technology that is truly manufacturable. Carbon nanotube technology has shown promise but also shows a number of limitations. This paper describes a new approach to field emission technology and a route to manufacture. Conventional FEDs utilise the confining effects of electric fields at sharp fabricated microtips. It has been found that laser processed hydrogenated amorphous silicon shows remarkable field emission properties that can be readily exploited in display manufacture. Hydrogenated amorphous silicon after breakdown in an electric field forms filamentary regions that show stable field emission. The structure after breakdown, or conditioning, may have an inhomogeneous nano-scale granular structure. The filamentary channels can be determined by the distribution of the nano-particles and act as the source of emission. Gated filaments are a route to low voltage emission. This concept has been extended to form a two dimensional plane for field emission, but without the breakdown or conditioning step. The interaction of profiled excimer laser beams with thin films of hydrogenated amorphous silicon in contact with certain metals leads to surface roughening and the creation of nano particles. There is little confinement of the external field, yet large enhancement factors are found and emission is found at low thresholds and without hysteresis. The laser processing creates the conditions for a high internal electric field that is responsible for field emission. The uniform nature of the emission and the surface roughening effect makes the material a suitable candidate for simple fabrication of displays using materials and tools that are familiar to the industry. The laser processed material is coated with an insulator and metal and etched to form self aligned gated structures that extract electrons at low voltage. The electrons impinge on a phosphor plate through a vacuum space to form a display that is potentially superior to existing flat panel displays in terms of cost, speed and power consumption.

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Keywords: Field emission displays, Hydrogenated amorphous silicon, Laser processing

1. Introduction

The flat panel display is one of the most important technologies in today's market. The market is huge, some $100bn, and is based largely on the Active Matrix Liquid Crystal Display (AMLCD) technology. The LCD at first glance seems to have resolved the display problem and is a true mass market device. The most successful technology is based on amorphous silicon Thin Film Transistors (TFTs) and the cost of this mature technology have enabled an affordable technology for many applications. However, the technology has some limitations that are evident for particular applications such as true video rendering of images, and there is room for new technologies. Field Emission Displays (FED) have been studied for some years and have long been considered a candidate for the ideal display with its emissive nature, true colour, high speed and low power. Early devices exploited the geometric confinement of electric fields at sharp emitter micro-tips producing high local fields at low voltages. This allowed for quantum mechanical tunnelling of electrons from the emitter point into vacuum. The early devices were metallic structures, and were developed by Spindt as early as the 1960/70s, forming the foundation of the modern FED.

Silicon emitters have also been studied for some time. However, the expense, area limitations and uniformity issues have precluded their use. Many outstanding demonstrator devices were made that showed the technological superiority of the technology. However, the problem with all of these technologies has been in

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manufacture, and the complexity of forming large arrays has proved to be impossible.

More recent work has shown that it is possible to find low electric field emission in *planar* or flat thin film systems without the need to process micro-tip structures. The mechanism of field emission is still a matter of debate. Fowler and Nordheim derived a relationship between the current density and electric field based on electron tunnelling through a triangular barrier [1,2]. This enabled room temperature cold cathode emission with a fast field response at ~10MV/cm. However, for practical devices, high fields are enhanced by sharp features where local external field enhancement is generated.

Electron emission is governed by the Fowler-Nordheim expression which relates current density to work function and the applied electric field. The emission current can be simplified to:

$$I = \alpha E^2 \exp(-b\phi^{3/2}/\beta E)$$

where E is the applied field, ϕ the work function and β the field enhancement factor. Plotting a Fowler-Nordheim graph for most field emission sources provides a linear relationship, despite the radically different materials and structures. It is represented here simply to introduce the β-factor that becomes anomalously high in certain configurations.

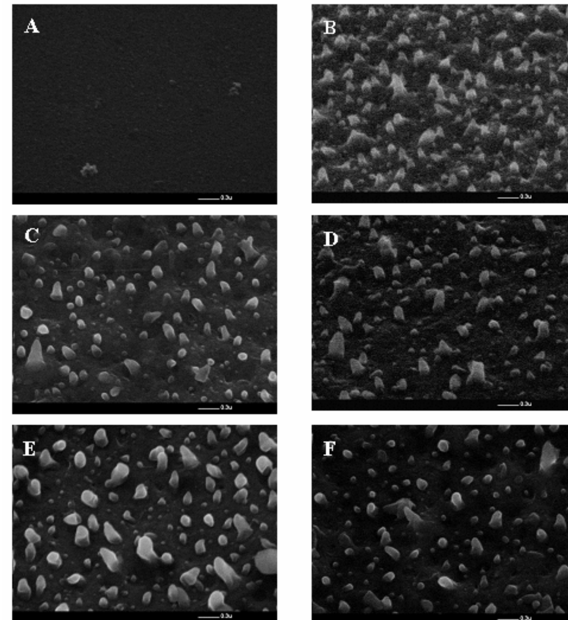
The early etched metallic structures uncovered many of the problems that plagued field emission. Successful arrays of emitters were realised practically by Spindt, who utilised microelectronics fabrication techniques [3]. Continued development of devices exposed the limitations of the technology where arcing, noise and adsorbate problems added to those in manufacturing large arrays. Upon their arrival, carbon nanotubes (CNTs) were soon seen as the perfect emitter, with their high aspect ratio and stability in electric fields, but proximity effects and stray dominant emitters made them difficult to control.

Recently, thin film planar systems have shown some promise. Carbon systems, other than CNT, have also shown promise, with emission measured in amorphous carbon [4], and diamond like carbon [5]. Silicon also has been studied using planar amorphous [4] and microcrystalline [6] silicon.

Much work has been carried out on filamentary conduction in ultra-thin amorphous silicon films [7-10] This work reported on stable devices that on application of an electric field, the as-deposited silicon films broke down by a so called ‘forming’ process. The resultant permanent filament created by electro-migration showed interesting effects with the high current densities, such as bistability, apparent quantised resistance and field emission. Silva *et al*. showed that by current stressing amorphous silicon, structural changes were observed that gave exceptionally low threshold voltage values for electron emission [4]. Laser processing to create micro-structural inhomogeneity was an attempt to distribute the filamentary behaviour of amorphous silicon across two dimensions and to see if gating filaments could go some way to providing a simple field emission system.

2. Laser processed thin film hydrogenated silicon

This study reviews the technology and presents some insights into the field emission process and the method of fabrication of a new display technology using multi-layers with little recourse to complex lithography and results from test structures, and introduces initial modelling studies of thermal and electrostatic effects and power consumption.



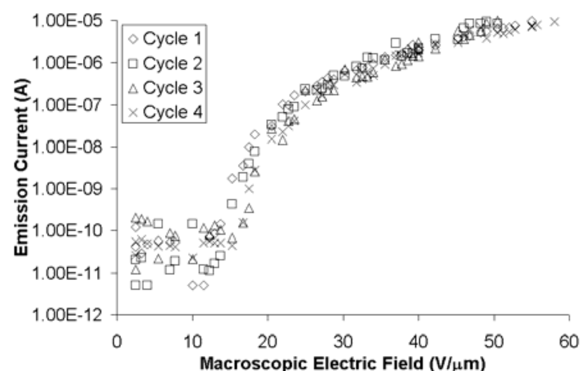


Fig. 1. Surface morphology of thin film silicon on exposure to 248nm excimer laser irradiation at 20ns, travelling at 1mm/sec. for varying energies (A) 179 mJ/cm², 204 mJ/cm², 221 mJ/cm², 235 mJ/cm², 241 mJ/cm², 263 mJ/cm² The plot of the emission current against electric field is for silicon at 200mJ/cm² and for this series is the only material with useful emission (after [11]).

Recently it has been shown that laser treatment of hydrogenated amorphous silicon produces a roughened surface that gives remarkable field emission properties [11]. Amorphous silicon grown under standard conditions for TFTs is deposited on metal covered glass substrates. Using a KrF excimer laser at a wavelength of 248nm, if the material is processed with its as-grown hydrogen

content of 10% and in air, the surface of the material is disrupted and 'conical' structures are produced. This surface is highly dependent on the laser energy, and on other parameters that are discussed below. If the device is mounted in vacuum, field emission measurements can be carried out on the material with no further processing. Low voltages can be applied, resulting in low threshold fields for emission. These emission properties cannot be described by geometric field enhancement considerations alone. It has been found, however, that the internal nanostructure of the material has a profound effect on the nature of electron emission, and this in turn can be determined by the laser parameters.

Undoped amorphous silicon was deposited for all tests by the plasma enhanced chemical vapour deposition (PECVD) method to a thickness of 100 nm using silane (SiH_4) with hydrogen dilution on to thin film molybdenum metal on glass, deposited by a d.c. sputtering process. The silicon hydrogen content was measured to be ~10%. No pre-baking or dehydrogenation steps were taken before the samples were exposed to the full selected value of laser energy. The KrF excimer laser used throughout this work delivered 20 ns pulses on a $1cm^2$ footprint to a moving substrate on a stage where the speed of traverse altered the effective frequency seen by the films. Field emission measurement was done using a spherical metallic anode probe, 5mm in diameter, movable by piezo-ceramic actuators in sub-micron steps, and with the samples mounted on an X-Y stage, again with controlled actuators. Measurements were generally carried out in vacuum better than 2x 10^{-6} mbar.

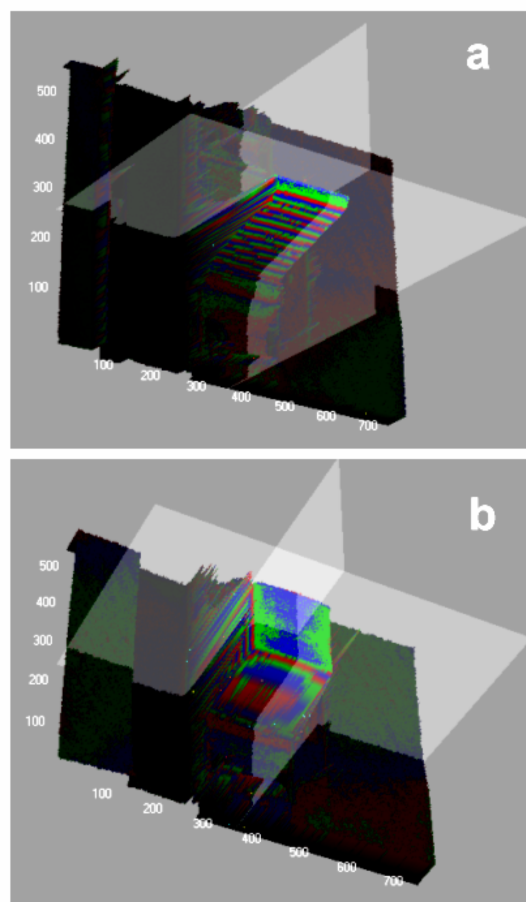


Fig. 2. 3D profiles of the laser footprint (1cm x 1cm) showing (a) the leading edge profile for controlled de-hydrogenation, (b) the top hat profile typical of the Low Temperature Polysilicon for the TFT process.

Once the thin film silicon was deposited, it was exposed to excimer laser radiation, with a shaped beam profile. The result is a surface roughened film that contains crystallised and metallic inclusions. This film now has the structure that enables field emission without further processing, conditioning or hysteresis. The surface has high uniformity of emission and imaging in phosphor revealed unprecedented uniformity (>80%). Such performance suggests a self-ballasting behaviour, possibly induced at the back contact interface by diffused metallic particles. The surface roughening predicts a geometric β-factor of ~3 (derived from the feature geometry relationship to the β-factor ~h/r with h the feature height and r the radius). However, *apparent* β-factors in excess of 500 are measured. The field emission plot in Fig. 1 shows the device characteristics with a threshold of 10V/µm (although thresholds < 2V/µm can be measured), with no hysteresis and uniformity and reproducibility for a number of scans.

The excimer laser pulse profile has a profound influence on the surface topography and field emission properties. The comparable low temperature polysilicon (LTPS) TFT fabrication method generally relies on a 'top

hat' laser profile processing de-hydrogenated silicon. In our case the hydrogen remains as the as-deposited content. Careful control of scan speed and beam shape gives a uniform distribution of microtips. The leading edge in Fig. 2(a) serves to de-hydrogenate the sample, giving some control of the ablation and crystallisation and feature size. Processing is done in air, and this too affects the structure and composition of the resultant material. The material when exposed to the desired energies is near the ablation limit, and sees temperatures high enough to melt the silicon (see thermal modelling below). After the first pulse, the silicon has melted and quenched, losing its hydrogen and altering the absorption coefficient, before it sees the second pulse of the sequence. This melt/quench cycle continues with each pulse, eventually forming a unique internal structure.

3. Device and Process Modelling

We have modelled the laser processing of thin film structures, using the COMSOL™ finite element multi-physics modelling package (COMSOL Ltd. Hatfield, Herts, UK). This allows us to examine the effects of varying laser fluence and film geometry on the heating, melting and re-solidification of silicon in device structures. Essentially, we can solve the heat transport equation whilst including known temperature variations of the thermal properties (C_p,*the specific heat capacity,* κ *the thermal conductivity*) of the substrate, metal contact and silicon film, as well as latent heat and phase changes. In addition, the time and depth variation of the laser optical energy absorption are included in the heat equation source term, as well as radiation loss from the film surface. Overall the complex interplay of many linked parameters and processes may be studied, so as to provide a useful guide to actual fabrication requirements.

Fig. 3 shows thermal time and depth profiles in a 100nm a-Si:H film on a 100nm Cr layer on 7059 glass substrate, for a representative KrF excimer laser fluence of 250 mJ at 248 nm wavelength, consisting of a single Gaussian pulse of FWHM = 20ns. The high 'spike' (in red) shows the region of melting obtained at this fluence. It is clear that for this case, melting has been extended to 60 nm depth. The visible plateau during cooling is associated with latent heat evolution.

Comsol™ has also been used to determine and optimize the pixel structures by analyzing ballistic electron transport in various device structures and configurations. Computer modelling of field distributions and particle ballistics in the FED structure allow us to examine and implement electrode designs which allow higher definition via

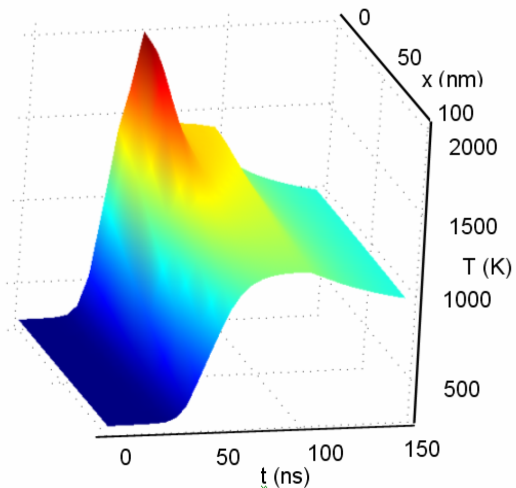


Fig. 3. Thermal time and depth profile in a 100nm a-Si:H film on a 100nm Cr layer on a 7059 glass substrate, for an excimer laser fluence of 250 mJ at 248 nm wavelength, consisting of a single Gaussian pulse of FWHM = 20ns, with a peak at 50ns from the time origin.

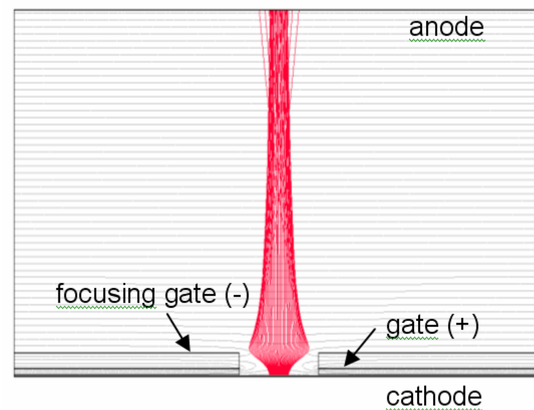


Fig. 4. Modelled beam profile for gated and focused sub-pixel structures using Comsol Multilab. Each pixel is fabricated with 300 – 1000 of these structures.

focusing of the emitted electrons from individual cathode emission sites. Fig. 4 shows a field and particle ballistics plot for a simple multilayer emitter design. Each pixel contains as many as a thousand of these beams, from thousands of emitter sites in each via. The process of fabricating devices informed by this modelling is given below.

4. Device fabrication and operation

The fabrication of field emission displays has long been the major impediment to adopting the technology. The complexity of structures and lithographic steps required for conventional field emission devices has prevented some truly innovative technologies with smart demonstrators from reaching the market. The planar device described here offers a route to easy manufacture

using the mature basis of the amorphous silicon industry, laser processing familiar to the LTPS process, and simple multilayer deposition, fabrication and etch techniques. The basic device is a vacuum sandwich, with a laser processed cathode, and an anode plate with patterned transparent metallic electrodes and rgb phosphors.

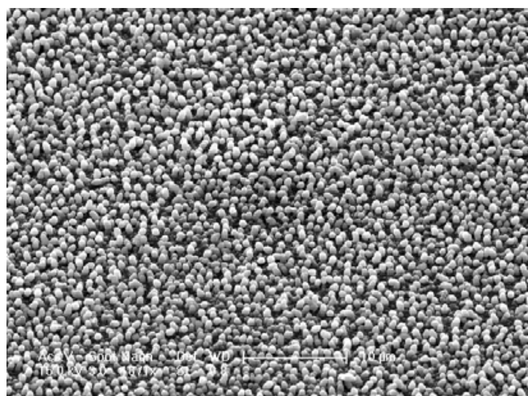


Fig. 5. Laser processed microtips coated in insulator 300 nm thick and capped with the metal that will eventually form the gate electrode.

The SEM pictures in Fig. 5 of laser processed thin film silicon in contact with thin catalytic metal show ‘microtip’ features that contain nanoscale inclusions. Application of the electric field allows proximity effects within the material to produce a very high internal electric field. The resultant ‘filamentary effect’ can be gated to give low voltage operation. Physically gating the features relies simply on coating them with an insulator and depositing the thin film metal gate on top, as shown in Fig. 5 above (and in more detail in 6(a)).

The material used as the gate insulator can be silicon nitride, as used for TFTs. However, we have been exploring the use of photo-patternable epoxy based materials such as SU-8 and utilizing their ease of fabrication and insulating properties. The material can be used to provide a conformal coating or as a planarizing agent. The material is spun or sprayed on, to a thickness of a few hundred nanometers, where this thickness will define the distance of the gate from the emitter and determine the operating voltage. Processing in this way produces ‘cocoon’ structures that need to be opened to expose the underlying emitter. However, it is not done at this stage of the process. Rather, the rest of the cathode device is put in place. This again uses SU-8 material, deposited to a thickness of a few to many microns, to define a spacer that will allow focusing of the electron beam.

The first step before SU-8 coating is dehydration; samples are pre-baked at 180°C for at least 30 min. They are cooled down to room temperature and immediately spin coated with photoresist at 3000 RPM for 30sec. In our case, for the gate insulating layer, we spin coat 0.4μm of SU-8 on top of the laser processed silicon sample. The next step is soft baking on a hot plate at 95°C for 2 min. After soft baking, it is UV exposed for 15 secs using a Carl SUSS MJB3 mask aligner. Hard baking follows at 95°C for 5 min and the sample is developed to remove all unnecessary photoresist. After developing, samples are rinsed in IPA and the device is ready for the final hard bake at 180°C for 1 hour. The gate metal (Mo, Cr) layer is deposited on top of the insulating SU-8 film and patterned, and then another thick (>2000nm) layer of SU-8 is deposited for supporting the aluminium top focusing electrode. The focusing electrode contains an array of holes as a path for the electrons from the emitting silicon cathode layer. The next step is SU-8 etching through the holes by means of ICP (Inductive Coupled Plasma) etching in an RF plasma using a mixture of oxygen and CF_4 gases, flow rates are 39 and 10 sccm respectively, pressure during deposition is 10 mTorr, substrate temperature 10°C. Reactive ion species will etch the thick SU-8 layer first and then the gate metal layer and last the thin layer of SU-8 on top of the emitting silicon film. Etching rates for SU-8 and Mo are typically 650nm/min and 80nm/min.

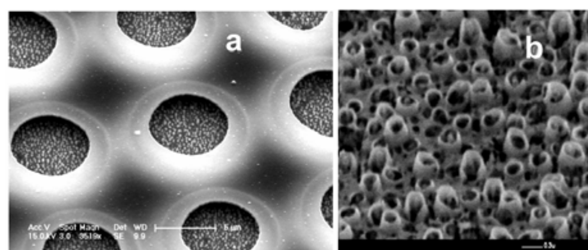


Fig. 6. (a) Part of the focusing array within a single pixel (300 – 1000 in each pixel) showing the underlying encapsulated emitters and (b) an electron micrograph of the emitters after etching to expose the micro-tips.

The simple multilayer sequence of fabrication allows a ‘top down’ lithography process, where holes are defined in the top aluminium metal within each pixel that will eventually act as a focusing ring for the beam of electrons and keep them confined to the pixel, avoiding cross talk. The focusing ring then acts as a mask for the etching of the SU-8 insulator down to the metal gate line. The device is then ready to have the gate metal etched to expose the micro-emitter structures. Fig. 6(a) shows the effect of etching in a dilute oxygen plasma after exposing a via through the aluminium focusing grid down to the gate metal layer. The etch conditions are then altered to bombard the gate metal by energetic ions, aided by enhanced surface activity through field confinement at the tip in the plasma field. Fig. 6(b) is a magnified picture of the individual emitters exposed by this process of eroding the metal and the encapsulating insulator, giving a gate to emitter distance of less than 0.5μm (determined by the gate insulator thickness).

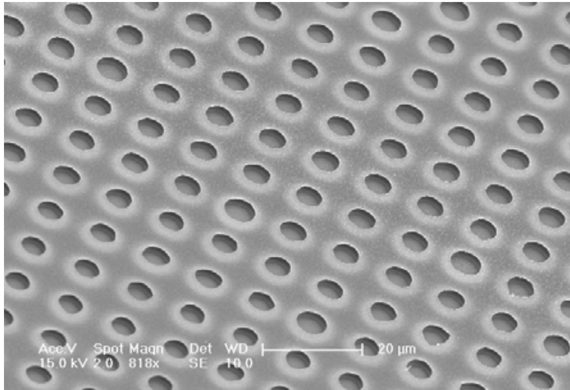


Fig. 7. Electron micrograph of the surface of a completed pixel structure.

Each pixel in the display is made up of hundreds or thousands of focusing sub-elements depending on the resolution of the display. Fig. 7 shows a part of a single pixel that emits focused beams to the anode plate.

5. Power consumption considerations

As we face global changes with fears of energy supply security and climate change, the electronics industry is striving to address power issues in devices. Power use by electronic devices is a major issue in terms of current energy problems, CO_2 emissions and climate change. It is also a crucial parameter in the new age of converging computing and displays in mobile computers and communication devices. The LCD flat panel display has enabled this convergence, and notebook computers hold an important place in the market. The move from CRT to LCD has provided a considerable advantage, but more demands are now put on the display to provide longer battery lifetime and more power for key processors.

The emissive nature, and the fast response time of the phosphor, makes the FED an inherently more efficient display than competitors. Power consumption in a portable display system is a main concern as it reduces battery lifetime, impacts circuit reliability, and generates heat. The FED is an emissive display that has natural advantages over existing flat panel displays such as AMLCD. As it is emissive, power is consumed only when a pixel is selected and illuminated. This can be determined to some extent by the fast speed of the phosphor. The driver electronics of the FED are responsible for addressing and controlling the matrix of pixels that compose the image. To perform this addressing function, modern flat panel display electronics can consume up to one-third of the power dissipation. The power dissipation in the display electronics has therefore emerged as an important aspect of the FED panel and subsystem. Our aim is to develop low-power row and column driver circuits based upon the specific functional requirements of the field emission display and the ability to implement gray scale.

In order to conduct a comparison for FED power consumptions for a panel which is 10” (6.2 x 8.3 inch), VGA (640 x 480) operating at 4kV with an overall luminance of 200 cd/m^2, and a luminous efficacy of 10 lm/W; the pixel current can be estimated via the luminance as:

$$L = V\,I\,D_c\,\varepsilon / \pi\,A\,,$$

which implies the current to be given by:

$$I = L\,\varepsilon\,A / V\,D_c\,\pi\,.$$

The duty cycle, dc, is 1/480, giving a current of 0.252 A. The pixel current is thus 0.3 μA per pixel. Due to voltage drops at the emitters and luminous efficacy corrections, a 10-100 fold increase in the current maybe required in practice. This increases the pixel currents to between 3 and 30 μA, which is in good agreement with literature values for FEDs. But, using this scenario we can now model the data and compare the results with those for typical LCD and plasma display panels. The maximum brightness is assumed to be 500 cd/m^2. The average pixel level (ω_{APL}) is defined as the time average of the video signal input voltage to the TV set, and is usually expressed as a percentage of the full white signal level voltage and has major impact on TV power usage. According to actual measurements, ω_{APL} is assumed to be 20% in the following analysis. The video refresh rate is 60 Hz. For 42 inch displays, the width (*W*) is 36.6 inch (93 cm), and the height (*H*) is 20.6 inch (52.3 cm).

Common parameters	L_{max}	ω_{APL}	f_F	Format: M×N
Value	1000 cd/m^2	10-50%	60 Hz	XGA: 1024×768

5.1 Liquid Crystal Display (LCD)

The power consumption in LCD panels is mainly composed of the backlight power P_{BL}:

$$P_{BL} = \frac{L_{max} \cdot \pi \cdot H \cdot W}{\varepsilon_{BL} \cdot \gamma_{ls} \cdot \eta_{ap}}$$

where ε_{BL} is the total efficiency of the backlight system, γ_{ls} is the light source efficacy and η_{ap} is the aperture ratio of the pixel. The relative values are shown below??.

LCD parameters	ε_{BL}	γ_{ls}	η_{ap}
Value	2 %	60 lm/W	80 %

5.2 Plasma Display Panel (PDP)

The power consumption in PDPs is mainly from the sustain power $P_{sustain}$:

$$P_{sustain} = \frac{2\omega_{APL} \cdot G \cdot C_{sustain} \cdot V_{sustain}^2 \cdot f_F \cdot (3 \cdot M \cdot N)}{\varepsilon_{dc}}$$

where G is the gray-scale, C_{sustain} is the sustain capacitance, V_{sustain} is the sustain voltage and ε_{dc} is PDP discharge efficacy.

PDP parameters	G	C_{sustain}	V_{sustain}	ε_{dc}
Value	256	55 fF	150 V	6%

5.3 Field Emission Display (FED)

The power consumption in a FED panel is from the FE device:

$$P_{FEDev} = \frac{\pi \cdot \omega_{APL} \cdot L_{\max} \cdot W \cdot H}{\alpha \cdot \varepsilon_{ph}}$$

where α is the ratio of the anode power to the cathode emission power, and ε_{ph} is the phosphor efficacy.

FED parameters	α	ε_{ph}
Value	60%	10 lm/W

We can compare these technologies to the test devices that have been described above extrapolated to a 10" VGA display. The power for such a device can be estimated (for an anode technology not yet optimised, and which should be improved by factor of 2 or 3 using optimized phosphors) to give a power consumption <10W**.**

The fast response time and low power consumption are key elements of a modern display technology. When this is coupled with ease of fabrication, conventional processing tools and the material that revolutionized displays to become mainstream devices, and an existing infrastructure it forms an interesting new technology.

6. Conclusions

Field emission display development has been plagued by difficulties in processing complex structures. However, it is still an appealing technology, despite considerable advances in liquid crystal technology, the current market leader. The aim of this work was to find a manufacturable solution to the FED problem. FED still promises the technological advantages of an emissive display. The laser processing of amorphous silicon approach adopted here has the added advantage of using a material that is already familiar to the display industry and uses tools that are available for current technology. The real benefit, however, is the ease of fabrication and the promise of a manufacturable device at low cost.

The laser processing is central to the final field emission properties of the material. The disrupted material with a surface morphology that is readily gated is easily controlled and produces an internal nano-structure that creates a high internal field. This is turn appears to produce 'virtual nano-wires' or filaments on the application of the external field. The lack of hysteresis is unusual for a thin film system and the apparent relative insensitivity to adsorbates an advantage. The underlying mechanism of field emission in this material is still not fully understood and is unusual. However, as a technology it has many potential benefits and offers a route to a successful low power field emission technology.

References

[1] R. H. Fowler, L. W. Nordheim, Proc. Royal Soc. A (**121**) 626 (1928).
[2] L. W. Nordheim, Proc. Royal Soc. A **121,** 626 (1928).
[3] C. A. Spindt, J. Appl. Phys. **39**, 3504 (1968).
[4] S. Silva, J. Vac. Sci. Tech. B **17** 596 (1999).
[5] G. Amaratunga, S. R. P. Silva, Appl. Phys. Lett. **68**, 2529 (1996).
[6] Y. F. Tang, S. R. P. Silva, J. Shannon, M. J. Rose, Appl. Phys. Lett. **80**, 4145 (2002).
[7] J. Hajto, A. E. Owen, A. J. Snell, P. G. LeComber, M. J. Rose, Phil. Mag. B **63**, 349 (1991).
[8] A. E. Owen, P. G. LeComber, A. J. Snell, M. J. Rose, J. Hajto, J. Non Cryst. Sol, **137-138**, 1257 (1991).
[9] J. Hajto, A. E. Owen, S. M. Gage, A. J. Snell, P. G. LeComber, M. J. Rose, Phys. Rev. Lett.

66, 1918 (1991).
[10] J. Hu, J. Hajto, M. J. Rose, A. J. Snell, Transactions on Electronics Vol. E84C(9) 1197 (2001).
[11] Y. Tang, S. R. P. Silva, B. O. Boscovic, J. Shannon, M. J. Rose, App. Phys. Lett. **80**, 4154 (2002).

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