Modeling of carriers mobility impact on CNT FET current-voltage characteristics

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In this paper, field effect transistor with active area made of carbon nano tubes (CNT FET), is investigated. At the beginning, CNT characteristics, structure and possibilities of their implementation as a FET channel, are presented. The new model of CNT FET current-voltage characteristics is developed and presented. In the model, capacitances of all interfaces are included. Special segment of this model is carrier's mobility model. Modeling of carrier's mobility is exposed. Two different carriers' mobility models are presented: analytical model that is developed and proposed and empirical model that is introduced. All models are modular and relatively simple. The results obtained by using proposed models are in very good agreement with already known ones.

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1. Introduction

Standard and widely used electron components made of silicon, slowly but surely, reach technical limits. These components will be replaced with new and better ones which have to be smaller, faster and consume less energy. The important goal is to obtain low cost complex functions device. To achieve this, new concepts are investigated. Implementation of new materials and structures are one of the solutions that can be used for improving electron component performances.

Electron components made of silicon-carbide (SiC) can be very good solution for high-power applications. They can be used for devices which have to operate under extreme conditions (e. g. high-temperature and high-radiation). SiC can be recommended as a material that can be used for fabrication of high-frequency components [1 - 9]. SiC based components have superior switching characteristics in comparison with the silicon ones. Their sizes are nearly twenty times smaller than corresponding silicon [2]. Benefits of using silicon doped by carbide, instead of standard pure silicon, for electron components production, are reflected in higher operating temperatures, better heat dissipation, wide margins, smaller sizes etc. It is worth to mention that SiC can be thermally oxidized to produce SiO_2. Thus, a variety of FET (Field Effect Transistor) structures in the material is possible to fabricate.

Heterostructural semiconductor components are expected to be high performances devices. Heterostructure Field Effect Transistor (HFET) has better and even new characteristics in comparison with standard silicon FET. HFET is known as high-speed and high-frequency device. Like other heterostructure devices, HFET consists of very thin layers of different semiconductor materials. Differences in band gap values of each material (layer), as well as differences in dopant concentrations of each layer, results in the quantum well appearance. Carriers confined in a quantum well form a Two-Dimensional Electron Gas (2DEG). Quantum well with 2DEG is, in fact, transistor's active area – channel. HFET's current is defined by charges which are reliced from the quantum well (controlled by gate voltage). [10, 14, 15].

Next step of carbide implementation in silicon electron components could be using carbon nanotubes (CNTs), as the structure which can be used as a FET's active area. Implementation of carbon nanotubes in silicon FET can be recognized as a realization of the heterostructure device. CNT based FETs can be observed as ultra high-speed and ultra low-power devices [11 - 13].

2. CNT structure and its implementation as a fet's channel

CNT are planar graphite sheets (graphene) which are wrapped into tubes. Different CNT structures can be fabricated. The electrical characteristics of CNT vary with its diameter and the wrapping angle of graphene. Because of very good electrical, thermal and mechanical characteristics, carbon nanotubes are very promising material for electron device applications today. CNTs have very high carriers' mobilities for the low electric field values. Drift electron velocities peak can be nearly five times higher than in silicon. CNTs can be doped by donors and acceptors [13]. It is indicated that CNTs could be used for making devices with large transconductances and high currents [13, 17] In order to improve the characteristics of standard Si transistor, active silicon area can be replaced with CNT.

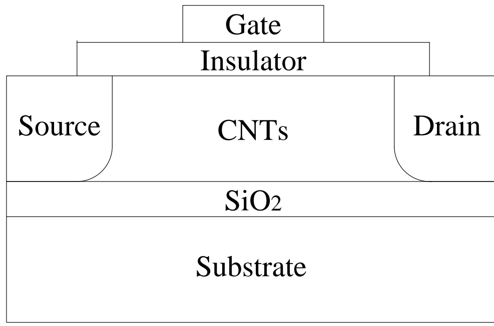

Fig. 1. CNT FET cross section.

A few of implemented nanotubes that are connected, at the same time, with source and drain area would form transistor's channel. Cross section view of a CNT FET is shown in figure 1. CNTs when used as a FET channel, can change the conductivity by a factor of a hundred or more.

3. Modeling of CNT FETs current-voltage characteristics

In CNT FETs, layer of nanotubes, which forms the active area, is observed as a conductive channel. Width of the channel is W and length is L. Modeling of CNT FET's current-voltage characteristics can be started with the well known drift-diffusion equation for the current density of electrons J_n:

$$J_n = Q_e \cdot n \cdot \mu_n \cdot E + Q_e \cdot D_n \cdot \frac{dn}{dx} \tag{1}$$

where Q_e is the electron charge, n is the concentration of electrons, μ_n is the electron mobility, E is the electric field, D_n is the constatnt and x is the direction of the current flow (the lateral direction in a plain transistor). Carriers concentration and mobility depend on temperature and applied electric field. On the other hand, carriers concentration, electric field and carriers mobility varies in the channel depending on possition. Taking these facts into account, the expression for the elementary drain current can be written more precise, as in [3 - 5], [10]:

$$\begin{aligned} dI_D = Q_e \cdot n\left(x,y,E_{CNT}\left(x,y\right),T\right) \cdot \mu_{CNT}\left(x,y,E_{CNT}\left(x,y\right),T\right) \cdot \\ \cdot E_{CNT}\left(x,y\right) \cdot W \cdot dy + Q_e \cdot D_n \cdot \frac{\partial n_{CNT}\left(x,y,E_{CNT}\left(x,y\right),T\right)}{\partial x} \cdot W \cdot dy \end{aligned} \tag{2}$$

In equation (2) E_{CNT} is the electric field in CNT (channel), μ_{CNT} is the carriers mobility in CNT, T is the temperature, x and y are the lateral and the vertical coordinate (possition in CNT channel).

Total drain current can be determined by integrating over the vertical axis:

$$\begin{aligned} I_D = Q_e \cdot \frac{\partial V_{CNT}\left(x,y\right)}{\partial x} \cdot W \cdot \\ \cdot \int_0^{y_{\max}} \begin{pmatrix} n\left(x,y,V_{CNT}(x,y),T\right) \cdot \\ \cdot \mu_{CNT}\left(x,y,V_{CNT}(x,y),T\right) \end{pmatrix} \cdot dy + \\ + Q_e \cdot D_n \cdot W \cdot \int_0^{y_{\max}} \frac{\partial n\left(x,y,V_{CNT}(x,y),T\right)}{\partial x} \cdot dy \end{aligned} \tag{3}$$

In equation (3), well known relation between the field E and potential V is used: E_x = -dV/dx. Realistic assumption in microelectronic, especially nanoelectronic devices domain is assumed: the variations of the electric field over the vertical axis, within the channel, are very small.

With the assumption that the carriers mobility in the active area (CNT channel) is constant and carriers concentration decreases lineary (short channel), equation (3) can easily be solved:

$$\begin{aligned} I_D = Q_e \cdot \frac{dV_{CNT}\left(x\right)}{dx} \cdot W \cdot n\left(V_{CNT}(x),T\right) \cdot \\ \cdot \mu_{CNT}\left(V_{CNT}(x),T\right) \cdot y_{\max} - Q_e \cdot D_n \cdot W \cdot n_{slope} \cdot y_{\max} \end{aligned} \tag{4}$$

or:

$$\begin{aligned} \left(I_D + Q_e D_n W n_{slope} y_{\max}\right) dx = \\ = Q_e W n\left(V_{CNT}(x),T\right) \mu_{CNT}\left(V_{CNT}(x),T\right) y_{\max} dV \end{aligned} \tag{5}$$

Integrating (5) along the channel, it is obtained:

$$\begin{aligned} \left(I_D + Q_e D_n W n_{slope} y_{\max}\right) L = Q_e W n\left(V_{CNTaver},T\right) \cdot \\ \cdot \mu_{CNT}\left(V_{CNTaver},T\right) y_{\max} \cdot \int_{V_S}^{V_D} dV \end{aligned} \tag{6}$$

In equation (6) L is the length of the CNT (channel), $V_{CNTaver}$ is the average voltage value in CNT's channel, V_S is the source potential and V_D is the drain potential. Using elementary transformations, similar like in [6], with the assumption that carriers concentration in CNT region is constant, expression for drain current can be determined.

- In linear mode, drain current is:

$$\begin{aligned} I_D = \frac{\mu_{CNT}\left(V_{CNTaver},T\right) \cdot C_{eq}^{/} \cdot W}{L} \cdot \\ \cdot \left(V_{GS} - V_{Th} - \frac{V_{DS}}{2}\right) \cdot V_{DS} \end{aligned} \tag{7}$$

- In saturation mode, drain current is:

$$I_D = \frac{1}{2} \frac{\mu_{CNT}\left(V_{CNTaver},T\right) \cdot C_{eq}^{/} \cdot W}{L} \cdot \left(V_{GS} - V_{Th}\right)^2 \tag{8}$$

In expressions (7) and (8) V_{GS} is the gate to source voltage, V_{th} is the threshold voltage, V_{DS} is the drain to source voltage and $C_{eq}^{/}$ is the equivalent capacitance per unit area.

In CNT FET exist few interfaces with their own capacitances: source C_S, gate C_G, drain C_D and substrate C_{substr}.

Gate to channel capacitance C_G can be calculated as:

$$C_G = C_{ox} = \varepsilon_0 \varepsilon_{r1} \cdot \frac{W \cdot L}{t} \tag{9}$$

t is the gate – channel separation or gate insulator thickness, ε_0 is the permittivity and ε_{r1} is the relative permittivity of the gate

Other mentioned capacitances (between terminals) can be calculated as [18, 19]:

$$C_S = 0.097 C_{ox} \tag{10}$$

$$C_D = 0.040 C_{ox} \tag{11}$$

$$C_{substr} = \varepsilon_0 \varepsilon_{r2} \cdot \frac{W \cdot L}{t_{SiO_2}} \tag{12}$$

Charge stored in those capacitances is:

$$Q = C_S V_S + C_G V_G + C_D V_D + C_{sub} V_{sub} \tag{13}$$

Equivalent gate to substrate capacitance is:

$$C_{G-sub} = \left(\frac{1}{C_G} + \frac{1}{C_{sub}} \right)^{-1} \tag{14}$$

Equivalent source to drain capacitance is:

$$C_{S-D} = \left(\frac{1}{C_S} + \frac{1}{C_D} \right)^{-1} \tag{15}$$

Equivalent capacitance C_{eq} depends on gate to substrate and source to drain capacitances.

4. Modeling of CNT FETs carriers mobility

4.1 The first (analytical) model

Carriers mobility is dependent on temperature and can be described by:

$$\mu(T_{CNT}) = \mu(T_a) \cdot (\frac{T_a}{T_{CNT}})^{\alpha} \tag{16}$$

In equation (16) T_a is the ambient temperature, T_{CNT} is the temperature of the active area of CNT FET and α=1.5.

The carrier mobility dependence on electric field is given by [5]:

$$\mu(E) = \frac{\mu_0}{1 + \left| \frac{E}{E_{crit}} \right|^{\lambda}} \tag{17}$$

where μ_0 is the mobility for the low intensity electric fields, E is the electric field in a CNT channel, E_{crit} is the critical value of the electric field and λ is the constant witch is different for electrons and for holes (for electrons: λ=1.6, for holes: λ=1.1).

Transport in the CNTs, thanks to their structure, is almost strictly lateral, and carriers mobility degradation is caused dominantely by the vertical electric field component. Considering only the vertical component of the electric field E_{CNTy}, equation (17) can be rewritten as:

$$\mu_{CNT}{}' \left(E_{CNT} \right) = \frac{\mu_0}{1 + \left| \frac{E_{CNTy}}{E_{ycrit}} \right|^{\lambda}} \tag{18}$$

The vertical component of the electric field's critical value is, in SiC based electron components, for electrons: E_{ycrit}=0.6MV/cm and for holes E_{ycrit}=0.7MV/cm.

Baering in mind that for the low values of electric field, temperature has the dominant influence on the carriers mobility, analytical model for the carriers mobility can be written as:

$$\mu_{CNT} \left(E_{CNT}, T_{CNT} \right) = \frac{\mu(T_a) \cdot \left(\frac{T_a}{T_{CNT}} \right)^{\alpha}}{1 + \left| \frac{E_{CNTy}}{E_{ycrit}} \right|^{\lambda}} \tag{19}$$

Introducing proposed model (19) into (14) and (15), final CNT FET current-voltage model is obtained:

- in linear operating mode:

$$I_D = \frac{\frac{\mu(T_a) \cdot \left(\frac{T_a}{T_{CNT}} \right)^{\alpha}}{1 + \left| \frac{E_{CNTy}}{E_{ycrit}} \right|^{\lambda}} \cdot C_{eq}^{/} \cdot W}{L} \cdot \left(V_{GS} - V_{Th} - \frac{V_{DS}}{2} \right) \cdot V_{DS} \tag{20}$$

- in saturation mode:

$$I_D = \frac{1}{2} \frac{\dfrac{\mu(T_a)\cdot\left(\dfrac{T_a}{T}\right)^{\alpha}}{1+\left|\dfrac{E_{CNTy}}{E_{ycrit}}\right|^{\lambda}} \cdot C_{eq}^{/} \cdot W}{L} \cdot \left(V_{GS}-V_{Th}\right)^2 \qquad (21)$$

4.2 The second (hybride, analyticaly-empirical) model

The band structure splits into a system of subbands when graphene is wrapped into a CNT. Each of subbands has a characteristic carrier's mobility. Entire carrier's mobility can be expressed as:

$$\frac{1}{\mu_{CNT}\left(d_{CNT},E_{CNTaver}\right)} = \sum_k \frac{1}{\mu_{kCNT}\left(d_{CNT},E_{CNTaver}\right)} \qquad (22)$$

Drift velocity in the first zone is higher than drift velocity in the second zone. If two lowest subzones are taken into account, carriers mobility can be find from:

$$\frac{1}{\mu_{CNT}\left(d_{CNT},E_{CNTaver}\right)} = \\ = \frac{1}{\mu_1\left(d_{CNT},E_{CNTaver}\right)} + \frac{1}{\mu_2\left(d_{CNT},E_{CNTaver}\right)} \qquad (23)$$

where μ_1 and μ_2 are mobilities of the subzone 1 and subzone 2. Carrier's mobility of the first subzone can be modeled as in equations (17) or (18). The mobility at the low electric fields can be expressed by empirical equation:

$$\mu_0\left(d_{CNT}\right) = 40 d_{CNT}^{\;2}\left(1+\frac{\alpha}{d_{CNT}^{\;2/3}}\right) \qquad (24)$$

By introducing (24) into (17) and/or (18) hybrid mobility model for the first subzone is obtained.

The analytical model which is given by equation (19) can also be used for the first subzone carriers mobility modeling.

Second subzone mobility can be expressed as:

$$\mu_2\left(d_{CNT},E\right) = \frac{v_{d\max}\left(d_{CNT}\right)}{E_{CNTaver}\left(1+\dfrac{E_{CNTaver}}{90E_{crit}\left(d_{CNT}\right)}\right)} \qquad (25)$$

Empirical model can be used for the critical electric field (defined by the pick of the carriers drift velocity):

$$E_{crit}\left(d_{CNT}\right) = \frac{1}{d_{CNT}^{\;3/2}}\left(1+\frac{64\alpha}{d_{CNT}^{\;2}}\right) \qquad (26)$$

where diameter d_{CNT} and α are the parameters of CNT structure.

Maximal electron drift velocity v_{dmax} can be calculated from empirical model:

$$v_{d\max}\left(d_{CNT}\right) = 1.7\sqrt[3]{d_{CNT}}\left(1+\frac{\alpha}{2d_{CNT}}\right) \qquad (27)$$

By introducing (23) into (14) and (15), second CNT FET current-voltage model can be obtained:

- in linear operating mode:

$$I_D = \frac{\mu_{CNT}\left(d_{CNT},E_{CNTaver}\right)\cdot C_{eq}^{/}\cdot W}{L}\cdot \\ \cdot\left(V_{GS}-V_{Th}-\frac{V_{DS}}{2}\right)\cdot V_{DS} \qquad (28)$$

- in saturation mode:

$$I_D = \frac{1}{2}\frac{\mu_{CNT}\left(d_{CNT},E_{CNTaver}\right)\cdot C_{eq}^{/}\cdot W}{L}\cdot \\ \cdot\left(V_{GS}-V_{Th}\right)^2 \qquad (29)$$

5. Results and discussion

Using the proposed CNT FET analytical models, simulations were performed. For some parameters, following values were used: capacitance per unit area C_{ox}=200[aF/μm^2], channel width W=40[nm]-70[nm], channel length L=30[nm]-50[nm], threshold voltage at room temperature V_{th}=0.3[V], T_a=300[K], $\mu(T_a)$=2000[cm^2/Vs], λ=1.6.

In Fig. 2. dependences of the drain current I_D on the drain to source voltage V_{DS}, where gate to source voltage V_{GS} is parameter, are shown. The second mobility model is incorporated in proposed current-voltage characteristics model (d_{CNT}=58). In Figures 3., 4. and 5. dependences of the drain current I_D on the drain to source voltage V_{DS}, where gate to source voltage V_{GS} is parameter, for different temperatures (T=300K, T=400K, T=500K), are shown. Drain to source voltage is varied between 0.5V and 1V. The first mobility analytical model is incorporated in proposed current voltage characteristics model.

In Fig. 6. dependences of the drain current I_D on the gate to source voltage V_{GS}, where gdrain to source voltage V_{DS} is parameter, are shown. The second mobility model is incorporated in proposed current-voltage characteristics model (d_{CNT}=58).

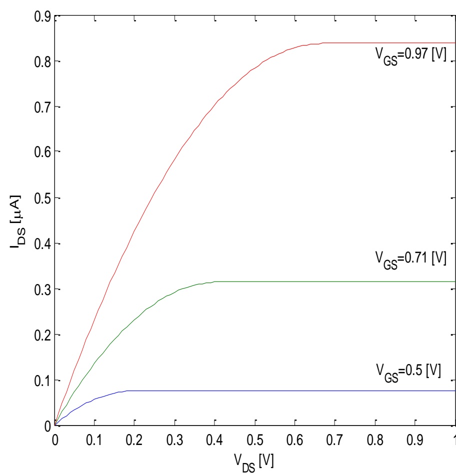

Fig. 2. Drain current I_{DS} versus drain to source voltage V_{DS}, for various values of gate to source voltages V_{GS} (Second mobility model, d_{CNT}=58).

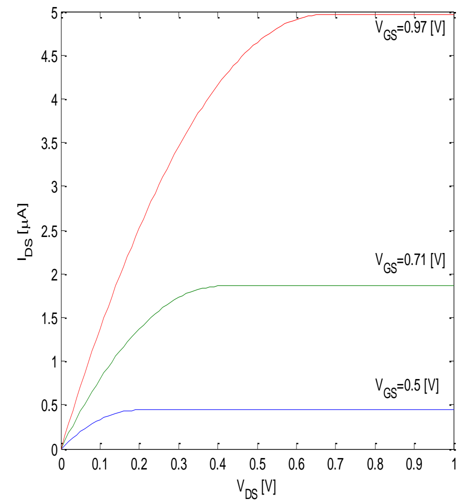

Fig. 5. Drain current I_{DS} versus drain to source voltage V_{DS}, for various values of gate to source voltages V_{GS}, T_{CNT}=500K.

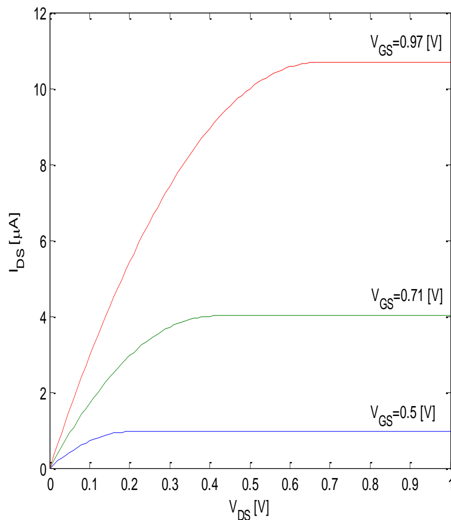

Fig. 3. Drain current I_{DS} versus drain to source voltage V_{DS}, for various values of gate to source voltages V_{GS}, T_{CNT}=300K

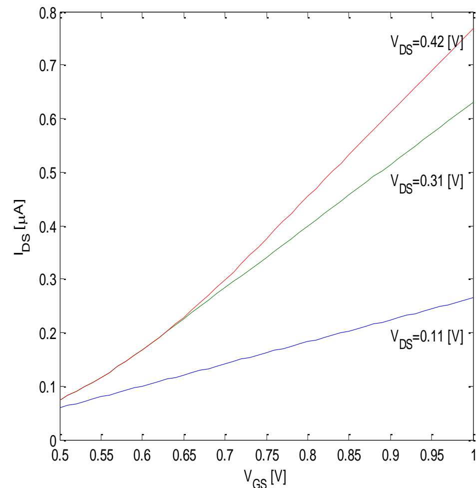

Fig. 6. Drain current I_{DS} versus gate to source voltage V_{GS}, for various values drain to source voltages V_{DS} (Second mobility model, d_{CNT}=58).

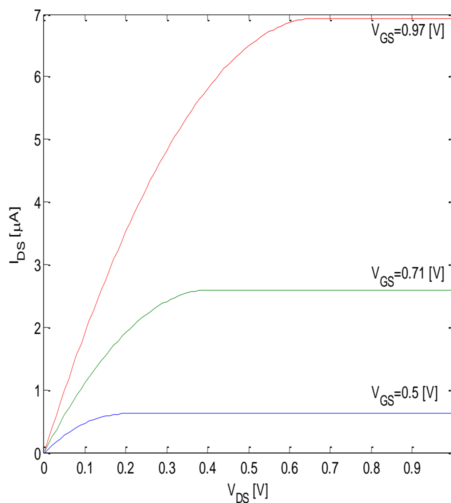

Fig. 4. Drain current I_{DS} versus drain to source voltage V_{DS}, for various values of gate to source voltages V_{GS}, T_{CNT}=400K.

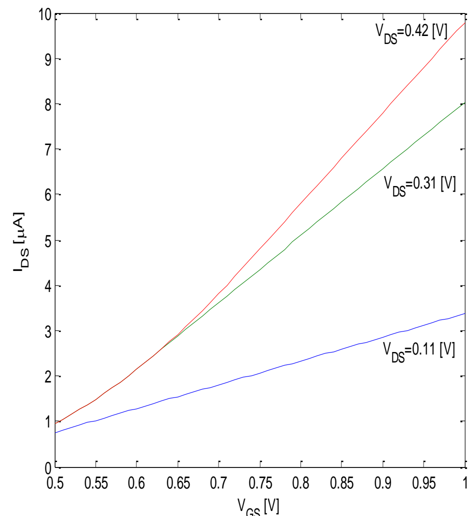

Fig. 7. Drain current I_{DS} versus gate to source voltage V_{GS}, for various values drain to source voltages V_{DS}, T_{CNT}=300K.

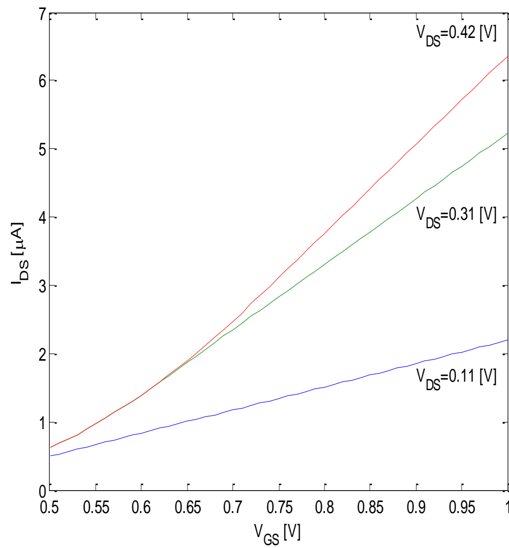

Fig. 8. Drain current I_{DS} versus gate to source voltage V_{GS}, for various values drain to source voltages V_{DS}, T_{CNT}=400K.

In Figs. 7., 8. and 9. dependences of the drain current I_D on the gate to source voltage V_{GS}, where drain to source voltage V_{DS} is parameter, for different temperatures (*T*=300K, *T*=400K, *T*=500K), are shown. The first mobility analytical model is incorporated in proposed current voltage characteristics model.

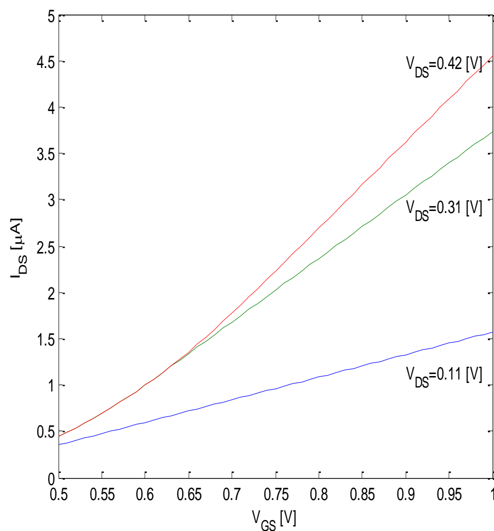

Fig. 9. Drain current I_{DS} versus gate to source voltage V_{GS}, for various values drain to source voltages V_{DS}, T_{CNT}=500K.

Drain current decreases when temperature increases. For temperature 300K, drain current is two times higher than that for 500K.

Shapes of the obtained curves are AS expected. Linear operating and saturation operating regime segments can be easily recognized on the figures. In linear operating regime, CNT FET's current increases with drain to source voltage as a square function, for fixed gate to source voltage. In saturation regime, drain current is constant (in fact, in experiments, it is almost constant). Drain current increases when gate to source voltage, which is parameter, increases. CNT FET's current increases with gate to source voltage as a square function, for fixed drain to source voltage.

Drift velocity maxima are about four time higher in CNT (v_{dmax} is almost 5x10^{7}cm/s for the long diameter CNT, (d_{CNT}=58) and 3x10^{7}cm/s for the small diameter CNT (d_{CNT}=10)) in comparison with standard semiconductor materials. Critical electric field is from 1kV/cm (the small diameter CNT) to 10kV/cm (the long diameter CNT).

Nanotubes dimensions have a significant impact on their characteristics. CNT can obtain significantly higher mobilities in comparison with the standard semiconductor materials. For d_{CNT}=58, the low fields mobility is 2x10^{5}cm^2/Vs, and for d_{CNT}=10 the mobility is approximately 4x10^{3}cm^2/Vs. Thus, high electron mobility can be achieved at low electric fields, if higher value diameter CNT is used.

Voltage and current values in the presented graphics are in good agreement with the values known from the literature.

6. Conclusion

The advantages of using carbon nanotubes, as FET's active area, are discused. CNT can achieve significantly higher mobilities in comparison with the standard semiconductors Two carriers' mobility models are exposed: the new analytical model and corrected empirical model. The new analytical model describes dependences of carriers mobility on applied electric field and temperature. For the low electric fields, temperature has dominant influence on the mobility and for high electric fields, such fields take the main role. Correction coeffitient, which describes carriers propagation through CNT FET's channel is introduced. The new analytical models of CNT FET current-voltage characteristics are also developed. Special attention is paid to capacitances of all interfaces. Developed carriers mobility models are incorporated into proposed CNT FET current-voltage characteristics model.

Using the proposed models, simulations were performed. The results obtained by using developed models are in very good agreement with already known and published ones.

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