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On the nature of the high-*k* dielectrics leakage current reduction by post-deposition annealing

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We have analyzed the newest reported in the literature experimental *I–V* characteristics of postdeposition annealed HfO_2 on silicon substrates, by employing a recently developed method for describing the leakage currents through high-κ/SiO_2 stacked structures, employed previously for Ta_2O_5. The presence of a very thin SiO_2-like interfacial layer between the HfO_2 and silicon and its effect on the leakage currents were explicitly included into calculations. Considering direct tunneling as a dominant conduction mechanism in SiO_2 and Poole-Frenkel emission in HfO_2, a satisfactory agreement with the experimental results was obtained. The possibility of some other current transport processes to be present in HfO_2 and the sensitivity of the method to detect them were also discussed. Based on the obtained results, it is argued that the interfacial SiO_2-like layer strongly influences the *I-V* characteristics of the HfO_2/SiO_2 structure. Experimentally observed reduction of the leakage currents after post-deposition annealing in different ambient (O_2, NH_3 and forming gas) of the structures, could be explained by the additional growth of the SiO_2–like interfacial layer, rather than by an improved stoichiometry of the bulk HfO_2.

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1. Introduction

The increasing demand for down-sizing of the Si devices has led to a significant reduction of the SiO_2 dielectric film thickness, currently reaching the value of 1.4 nm and below. Further reduction is restricted by high leakage current through the gate oxide as a result of quantum mechanical direct tunneling. Replacement of the conventional SiO_2 with a high permittivity (high-*k*) dielectric material is recognized as a promising approach for overcoming the problem [1]. Therefore, several metal oxides, such as HfO_2, ZrO_2, Ta_2O_5, TiO_2 or Al_2O_3, have been proposed and extensively studied. Every potential candidate for this role have to meet some criteria including high dielectric constant, low leakage current and good electrical properties of the high-*k*/Si interface [2]. In order to achieve better optimization of these parameters, different deposition techniques and postdeposition treatments have been studied. Postdeposition annealing of dielectric films is frequently employed procedure intended to improve the overall properties of dielectric films by improving the stoichiometry and microstructure of the bulk material as well as the interfacial region. Many authors have already reported its beneficial effects on the interface quality and leakage current characteristics of the high-*k* dielectrics on silicon [3-8]. A systematic study of the effects of postdeposition annealing in different chemistries on both the material and the electrical characteristics of HfO_2 films was recently reported by Puthenkovilakam *et al*. [9,10]. They found that annealing in O_2, NH_3 and forming gas results in a substantial growth of the interfacial layer, which resembles a SiO_2-rich dielectric layer. Concerning the electrical characteristics of the films, their results show that postdeposition annealing significantly reduces both the interface state density and the leakage current densities. The main goal of this work is to clarify the effect of leakage current reduction. As a starting point we used the observed correlation between the additional growth of the interfacial layer and the leakage current reduction. In order to investigate this correlation in as much as possible quantitative way, we made a theoretical modeling of the *I-V* characteristics reported in [10], taking into account the presence of the interfacial layer. It was done by employing the model previously developed for describing the leakage currents in Ta_2O_5/SiO_2 stacked structures on silicon [11,12].

2. Theory

The HfO_2 dielectric films are considered as composed of two homogeneous parts: a HfO_2 and a SiO_2-like layer. Under steady-state condition, the current density *J* through the system is independent on position, although it can be governed by completely different mechanisms in each layer. If we denote the current density through the HfO_2 layer as J_{hf}, and the corresponding current density through the interfacial layer as J_{if}, then it reads

$$J_{hf} = J_{if} . \quad (1)$$

Neglecting the space charge into the bulk of the layers, electric field in each layer can be considered as constant. Thus the voltage drops on the layers are

$$V_{hf} = d_{hf} E_{hf} \quad \text{and} \quad V_{if} = d_{if} E_{if} , \quad (2)$$

where d_{hf} and d_{if} are the thicknesses of the corresponding layers, and E_{hf} and E_{if} denote the electric fields in each layer. The total voltage drop over the dielectric stack is given by

$$V_{ox} = d_{hf} E_{hf} + d_{if} E_{if} . \quad (3)$$

By inserting the theoretical expressions for the current densities J_{hf} and J_{if} into Eq. (1), which will be discussed latter, the equation turns into the relation between the electric fields in the layers. Now, one should employ a numerical procedure for simultaneously solving Eqs. (1) and (3) to calculate the current density J through the system as a function of the voltage drop (V_{ox}) over the dielectric stack. Finally, the voltage drop (V_{ox}) has to be expressed by the gate voltage (V_g). They are related through the following equation [13]

$$V_{ox} = V_g - V_{fb} - V_s , \quad (4)$$

where V_{fb} is the flat-band voltage, and V_s is the voltage drop in the semiconductor.

The value of the flat-band voltage was determined by a standard method (not described here). To calculate the voltage drop in silicon (V_s), we used the following equation, which relates V_s with the electric field in the interfacial layer [14]

$$E_{if} = \pm \frac{\varepsilon_{Si}}{\varepsilon_{if}} \left(\frac{2kTp_0}{\varepsilon_{Si}} \right)^{1/2} \times \left[\left(e^{-\frac{qV_s}{kT}} + \frac{qV_s}{kT} - 1 \right) + \frac{n_i^2}{p_0^2} \left(e^{\frac{qV_s}{kT}} - \frac{qV_s}{kT} - 1 \right) \right]^{1/2} \quad (5)$$

where ε_{Si} and ε_{if} denote static dielectric permittivity of silicon and of SiO_2 respectively, p_0 is the equilibrium hole concentration in the bulk of the semiconductor, and n_i is the intrinsic carrier concentration of silicon. More detailed description of the model and the numerical procedure can be found elsewhere [12].

So far, we discussed the basic steps of the numerical procedure without concerning the issue of conduction mechanisms in the insulating layers. Now, we will focus on this issue. Generally, possible conduction mechanisms for the SiO_2 layer are the hopping conduction, which is typical for disordered materials, and direct or Fowler-Nordhaim tunneling enabled by the extremely small thickness of this layer.

The current density due to the hopping conduction is given by the following expression:

$$J_{hc} = \sigma_{if} E_{if} , \quad (6)$$

where σ_{if} is the temperature dependent hopping conductivity.

Direct tunneling current density through the SiO_2 layer is described by

$$J_{dt} = \frac{q^2}{8\pi h\phi} E_{if}^2 \times \exp\left[-\frac{8\pi\sqrt{2m^* q\phi}}{3hE_{if}} \left(1 - \left(1 - \frac{d_{if}}{\phi} E_{if} \right)^{3/2} \right) \right], \quad (7)$$

while the current density due to the Fowler-Nordheim injection by

$$J_{FN} = \frac{q^2}{8\pi h\phi} E_{if}^2 \exp\left(-\frac{8\pi\sqrt{2m^* q\phi^3}}{3hE_{if}} \right), \quad (8)$$

where q is the electron charge, h is the Planck's constant, m^* is the effective tunneling mass of the charge carriers injected from the silicon substrate, and ϕ is the tunneling barrier height. Tunneling currents through the SiO_2 layer can be created by electrons or holes. In the case of p-type silicon substrate and gate positively biased, tunneling currents are due to the electrons injected from the inversion layer of the substrate. When the gate is negatively biased, free electrons from the HfO_2 layer should create the electron tunneling current. Since their concentration there is negligible, this current is practically zero. Therefore, only tunneling of holes from the p-type silicon substrate can contribute to the tunneling current [11].

The total current through the SiO_2 layer is then

$$J_{if} = J_{hc} + \begin{cases} J_{td} & E_{if} \le \phi / d_{if} \\ J_{FN} & E_{if} \ge \phi / d_{if} \end{cases} . \quad (9)$$

In special cases, when the thickness of the SiO_2 layer is below 2 nm, direct tunneling becomes significant at relatively low voltages. For example, if we consider tunneling of holes and assume that $d_{if} = 1.9$ nm and $\phi = 4.7$ eV, the direct tunneling current density at $V_{if} = 0.3$ V will be about 100 $\mathrm{nA/cm^2}$. At the same time, the current density due to the hopping conduction will be lower than 0.1 $\mathrm{nA/cm^2}$. Hence, it turns out that for SiO_2 layers thinner than 2 nm, the hopping component of the current density in Eq. (7) could be ignored with no significant effect on the computational results. As the thicknesses of the interfacial layers in the considered samples were smaller than 2 nm, we dropped out this component during the calculations.

The issue of conduction mechanisms in HfO_2 is subtle. There is relatively small number of papers, which report on that subject. Generally, it is believed that defect-related processes, such as Poole-Frenkel emission [15,17], trap-assisted tunneling [16], or field-assisted tunneling of trapped electrons to the conduction band of dielectric [17], are responsible for leakage currents through HfO_2 films. In this work, for the HfO_2 layer we have considered the Poole-Frenkel emission.

The current density due to the Poole-Frenkel emission obeys the following equation

$$J_{\mathrm{PF}} = \sigma_{\mathrm{hf}}(0) E_{\mathrm{hf}} \exp\left(\frac{1}{rkT} \sqrt{\frac{q^3}{\pi \varepsilon_0 K_{\mathrm{H}}}} \sqrt{E_{\mathrm{hf}}} \right), \quad (10)$$

where $\sigma_{\mathrm{hf}}(0)$ is a temperature-dependent defect related constant having dimensions of conductivity, r is the degree of compensation, k is the Boltzmann constant, ε_0 is the dielectric permittivity in vacuum, and K_{H} is the optical frequency dielectric constant of HfO_2.

Because the thicknesses of the HfO_2 layers in the various samples ranged between 3 and 4 nm, thus giving rise to the possibility of tunneling currents, we made separate computations of the *I-V* characteristics assuming that the leakage currents through the HfO_2 layers are due to the tunneling of the electrons from the gate. Direct and Fowler-Nordheim tunneling currents through the HfO_2 layer are described with Eqs. (7) and (8) in which the symbols m^*, ϕ, d_{if} and E_{if} have to be replaced with the corresponding quantities for the HfO_2 layer.

During the computations, we fitted only those parameters that are not well determined. When the Pool-Frenkel emission was considered, we fitted the defect related constant ($\sigma_{\mathrm{hf}}(0)$) for HfO_2 which is technologically dependent parameter. In the second case, when tunneling mechanisms through the HfO_2 were supposed, we fitted the tunneling electron mass in HfO_2 and the Al/HfO_2 barrier height for electrons. These two parameters were fitted under the constraint to have the same values for all samples. The thickness of the SiO_2 layer was treated as a fitting parameter in both cases because the numerical model is extremely sensitive to its variations. It was fitted in restricted range close to the measured value. For all other parameters, the following typical values, taken from the literature, were used: $m_{\mathrm{h}}^* = 0.51 m_{\mathrm{e}}$ [18] - tunneling hole mass in SiO_2, where m_{e} denotes the mass of free electron; $K_H = n^2 = 3.06$ - optical frequency dielectric constant of HfO_2; $\phi_{\mathrm{h}} = 4.70$ eV [18]- tunneling barrier height for holes in SiO_2; and $r = 1$ - compensation factor (we consider Poole-Frenkel effect without compensation).

3. Results and discussion

3.1 Poole-Frenkel mechanism in HfO_2-layer:

Fig. 1 presents the comparison between the leakage currents calculated by the proposed model for gate negatively biased, and corresponding experimental results published in [10] for HfO_2 films deposited by atomic layer deposition technique on p-type Si(100) wafers and subjected to postdeposition annealing. The *I-V* characteristics of the films annealed in O_2 and forming gas containing 90% N_2 +10% H_2 (FD-H_2) are shown in Fig. 1(a), while those regarding to films annealed in NH_3 and forming gas containing 90% N_2 +10% D_2 (FG-D_2) are shown in Fig. 1(b). All metal-oxide-semiconductor devices contain evaporated Al as a top electrode. It should be noted that the *I-V* characteristics are presented in the form of leakage current density versus oxide voltage V_{ox}. For that purpose, the experimental results given in the *I-V*$_{\mathrm{g}}$ form were transformed into the *I-V*$_{\mathrm{ox}}$ form using the Eq. (4). All computations were done with the reported values for HfO_2 films thicknesses [10]. The obtained values of the fitting parameters are summarized in Table 1. For comparison, the thicknesses of the interfacial layers as measured by HRTEM [10] are also given in Table 1. It can be seen that the obtained values of the interfacial layer thicknesses are underestimated compared with the measured ones.

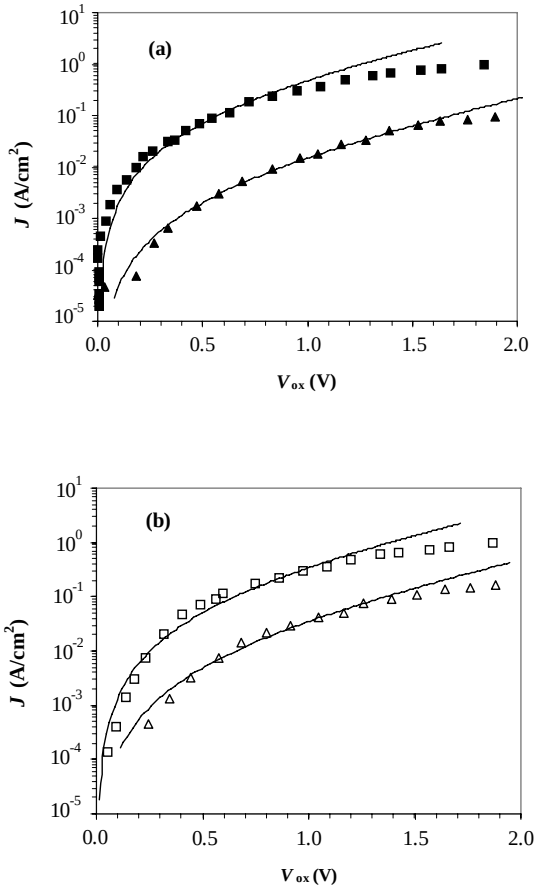

Fig. 1. Experimental I-V characteristics (negative gate bias) published in Ref. 10 for ***(a)*** *O_2-annealed (■) and FG-H_2 annealed (▲) films;* ***(b)*** *NH_3-annealed (□) and FG-D_2 annealed (Δ) films; compared to theoretical curves (solid lines).*

Even though the differences are not substantial (0.2÷0.3 nm), having in mind that the method is extremely sensitive to this parameter, it is worthwhile to take a closer look at these discrepancies. Namely, the voltage drop (V_{s}) in the semiconductor was calculated using Eq (5), which strictly speaking is correct only for a system in thermal equilibrium. For low current densities (of order of

1 nA/cm^2 or lower) we can still consider the free carriers in the silicon as to be in thermal equilibrium. Appearance of strong tunneling currents disturbs the equilibrium leading to reduction of the accumulated charge in near interface region of the silicon and decrease of the voltage drop V_s. As a result, the shift of the I-V_g curve toward the lower voltage region when converting it to the I-V_{ox} curve should be smaller.

Table 1.

Sample	$\sigma_{hf}(0)$ (Ω^{-1}cm^{-1})	d_{if} (fitted) (nm)	d_{if} (HRTEM) (nm)
O_2 annealed	8.2×10^{-7}	1.18	1.3
NH_3 annealed	8.2×10^{-7}	1.20	1.4
FG-H_2 annealed	1.2×10^{-10}	1.38	1.7
FG-D_2 annealed	5.5×10^{-10}	1.33	/

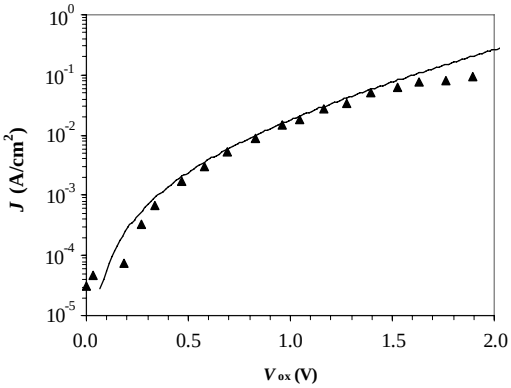

Fig. 2. Experimental I-V characteristic for FG-H_2 annealed film (▲) (negative gate bias, published in Ref. 10) compared to theoretical curve (solid line) obtained with modified defect related parameter for HfO_2 ($\sigma_{hf}(0) = 8.2\times10^{-7}\ \Omega^{-1}cm^{-1}$)

Hence, by using Eq. (5) one obtains higher value of current density for a given value of oxide voltage V_{ox} compared to the real one, which corresponds to thinner interfacial layer. To obtain a more accurate model that would take into account the nonequilibrium effects, both the Poisson equation and the current continuity equation have to be solved self-consistently in the near interface region of the silicon.

For the defect related constant in HfO_2 we found that it is about three orders of magnitude lower for the samples annealed in O_2 and NH_3 than the samples annealed in forming gases. In order to elucidate the influence of this parameter on the overall I-V characteristics of the stacked structures, we made computations in which its value was varied, keeping the thickness of the SiO_2 layer constant. Fig. 2 shows the fit for the film annealed in FG-H_2 when the value $8.2\cdot10^{-7}$ Ω^{-1}cm^{-1} is used instead of 1.2×10^{-10} Ω^{-1}cm^{-1}. Only a slight shift toward higher current densities is observed (about 0.01 A/cm^2 at 1.5 V). This indicates that in the studied range of gate voltages, the conductivity of the HfO_2 layer has no essential influence on I-V characteristics.

3.2 Tunneling of electrons through the HfO_2-layer

The results are not shown here because they are quite similar to the previous case. For the tunneling electron mass in HfO_2 and the Al/HfO_2 barrier height for electrons, we obtained the following values: $m_e^* = 0.08\,m_e$ and $\phi(\mathrm{Al/HfO_2}) = 1.30$ eV. They are in good agreement with the values reported in [15]. The obtained values for the thickness of the SiO_2 layers are presented in Table 2. They are very close to the fitted values given in Table 1 (differences are not bigger than 0.03 nm).

Table 2.

Sample	O_2 annealed	NH_3 annealed	FG-H_2 annealed	FG-D_2 annealed
d_{if} (nm)	1.15	1.18	1.38	1.33

These results put on an ambiguity about the dominant conduction mechanism in HfO_2. It could be resolved within the proposed model by analyzing the I-V characteristics for gate positively biased. If the Poole-Frenkel emission really dominates the current transport, then we will obtain the same values for the defect related constant $\sigma_{hf}(0)$ for both gate polarities, since the Poole-Frenkel effect is typically bulk limited mechanism. In contrary, if the curves for the cases of positive and negative gate cannot be fitted with the same values of this parameter, then it is most probably that the leakage currents through the HfO_2 layer for the case of negative gate are due to the tunneling of electrons and for the case of positive gate due to the Poole-Frenkel effect. It is to be noted that tunneling of electrons through the HfO_2 layer for the gate positively biased is excluded, because the HfO_2 layer is not in direct contact with the negative electrode (semiconductor). We did not analyze the I-V characteristics for gate positively biased because the corresponding experimental results published in [10] contain insufficient number of experimental points in the initial part of the curves important for the fitting procedure. After this initial part, the curves exhibit saturation of the leakage currents, which is a result of exhaustion of electrons in the inversion layer.

Although the ambiguity is not resolved at this time, we think that it is more likely the current in HfO_2 to be governed by the Poole-Frenkel emission than by tunneling processes, having in mind that:

- the results reported by Zhu *et al.* [15] for the HfO_2 films with similar thicknesses reveal that the leakage currents are temperature dependent, which rule out the possibility of pure tunneling mechanisms;
- as a result of very high trap density in HfO_2 films, it is likely that once the electrons enter the HfO_2 forbidden gap they become trapped after relatively short distance, continuing the transport by the Poole-Frenkel emission [12].

The obtained results reveal that leakage currents through HfO_2/SiO_2 stacked structures are strongly

influenced by the SiO_2 layer. The increase of its thickness from 1.18 nm for the O_2 annealed film to 1.38 nm for FG-H_2 annealed film results in decrease of the leakage current density for about 2 orders of magnitude. The leakage current density of the as-deposited film (not shown here), with thickness of 1 nm [10] was about 2 orders of magnitude higher than the one of the O_2 annealed film (1.18 nm). Hence, there is a quantitative agreement between the increase of SiO_2 layer thickness and the reduction of the leakage currents through the examined structures.

4. Conclusions

The previously developed model for describing the *I-V* characteristics of Ta_2O_5/SiO_2 stacked layers on silicon can be effectively employed for studying the leakage currents through HfO_2/SiO_2 structures, too. Although we found that both the Poole-Frenkel emission and tunneling of electrons from gate, when considered as conduction mechanisms in HfO_2-layer, lead to a satisfactory fit of the experimental results for gate negatively biased, we believe that Poole-Frenkel emission is more probable mechanism relying on the reasons stated above. However, the obtained values for the thickness of the SiO_2-layers are practically the same in both cases and are very close to the reported values in [10] measured by HRTEM. This means that the SiO_2 layer has a dominant influence on the leakage current characteristics in the studied range of voltages. The additional growth of the SiO_2-like layer induced by post-deposition annealing can account for the observed leakage current reduction.

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