Optical effects on the characteristics of a nanoscale SOI mosfet with vertical gaussian doping profile

K. GOWRI[a], M. ARUNACHALAM[b], V. RAJAMANI[c]
[a]*Department of Electronics and Communication Engineering, PSNA CET, Dindigul, Tamilnadu, India*
[b]*Department of Computer Science and Engineering, K.L.N College of Information Technology, Pottapalayam, Tamilnadu, India*
[c]*Department of ECE, Vel Tech Multi Tech Dr.Rangarajan Dr.Sakunthala Engineering college, Tamilnadu, India*

This paper deals with the effects of optical radiation of three dimensional nano scale SOI MOSFET with vertical gaussian doping profile including quantum mechanical effects. The model takes into account all the major effects that determine the device characteristics in the illuminated condition. The device characteristics are obtained using self-consistent solution of 3D Poisson–Schrodinger equations using Liebman's iteration method. Calculations are carried out to examine the effect of illumination on the surface potential, electric field, current-voltage characteristics and sub threshold characteristics. The obtained characteristics are used to examine the performance of the device for its suitable use as a photo detector in Opto-Electronic Integrated Circuit (OEIC) receivers.

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1. Introduction

Optoelectronic integrated circuits involve the integration of electronic and optical components and optical interconnects. Optics provides the inherent advantages of large bandwidth, parallelism and reconfigurable configurations. However, optics does not provide input-output isolation, as electronic devices do, and it may be difficult to focus multiple beams in a parallel system. It is therefore logical to couple electronic and photonic devices resulting in optoelectronic configuration. An important aspect of both optical communication systems and computing systems is the interconnect medium. Considering electrical interconnections, it provides large bandwidth and high speed data transmission, immunity to mutual interference and cross talk freedom from capacitive loading effects. The large bandwidth translates eventually to system size reduction, reduced system power and increased fan out capabilities.

Many researchers have already demonstrated the suitability of Field- Effect Transistors (FETs) in OEIC applications to be used as photo detectors due to their excellent photosensitivity and integrated circuit compatibility [1,2]. How ever when the device dimensions are scaled down, short-channel effects (SCEs) are expected to play a vital role on the device performance when control of the channel region by the gate is affected by electric field lines from source and drain. [3]. The SCEs degrade the controllability of the gate voltage on channel charge and cause the dependence of device characteristics, especially the threshold voltage, upon the reduction of channel length. Fully depleted (FD) silicon-on-insulator (SOI) MOSFETs have attracted considerable attention because of their superior short-channel immunity, drive current and ideal sub threshold characteristics [3,4]. Some two dimensional analytical models for threshold voltage of fully depleted and partially depleted SOI MOSFETs are presented recently [5-8]. In 2D models, it is almost impossible to deal analytically with certain problems like short channel effects or narrow width effects without resorting to some sort of assumptions or approximations. Krishna meel et al and G.Katti et al have proposed some three dimensional [9,10] analytical models to provide more insight into the device characteristics .

One of the fundamental assumptions in all the above discussed models is that the SOI film doping concentration is uniform. In practical devices, however, the doping is normally non-uniform and the impurity profiles in ion-implanted devices generally resemble a gaussian distribution with a maximum concentration at a project range R_p and with a standard project deviation σ_p [11]. Ravariu et al [12] derived 1-D threshold models for both partially depleted and FD SOI MOSFETs on films with Gaussian profile. However, they are just derived for long-channel devices. Sarvesh Dubey et al [13] demonstrated the threshold voltage variations against channel length for different device parameters .They had shown that the threshold voltage of a DG MOSFET can be well controlled by controlling only the profile parameters while maintaining other device parameters unchanged. Guohe Zhang [14] proposed a surface potential function model perpendicular to the channel for a FD SOI MOSFET with vertical Gaussian doping profile and thereby derived an analytical threshold voltage in which the 2-D effects in both SOI and buried-oxide layers were considered.

In our work, we assume that the lateral channel doping concentration is uniform, and the vertical channel is assumed to be a Gaussian distribution. Based on this approximation, the optical characteristics of nano scale SOI MOSFET are examined. In this paper, a self-consistent solution for three dimensional numerical model of SOI MOSFET photo detector having a Gaussian doping profile including quantum mechanical effects using Liebman's iteration method has been developed and presented. The numerical modeling is generally preferred over analytical modeling as it offers greater flexibility and capability to handle complex field operations. The prime focus is to obtain the device characteristics under illumination, by numerically solving the 3D Poisson-Schrodinger equations directly until self-consistency is achieved. Our work provides a simple but fairly accurate model suitable for use in integrated optoelectronic circuit simulation purposes.

2. Physics based modeling

The basic structure of an SOI MOSFET is illustrated in Fig. 1 [14] & 2.

The following are the geometrical parameters:

(1) Gate length (L_g): The physical gate length of SOI MOSFETs, defined by spacer gap.

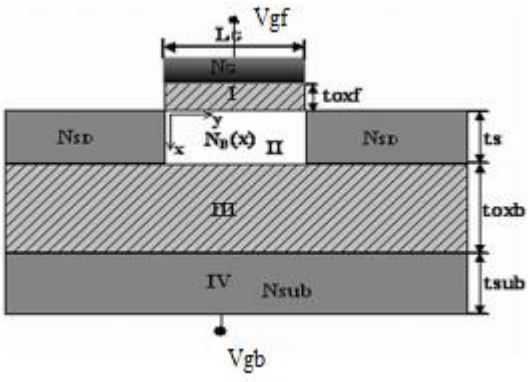

Fig.1. Cross section of fully depleted SOI MOSFET.

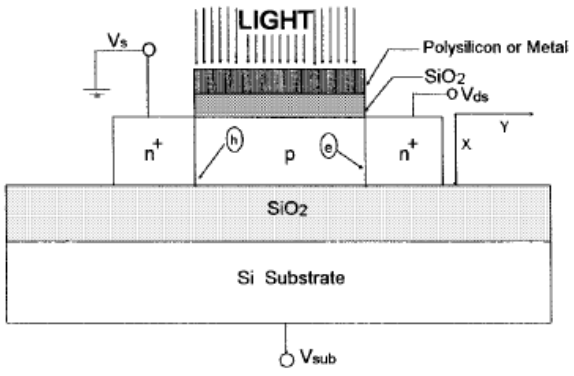

Fig. 2 Schematic diagram of SOI MOSFET under illumination.

(2) Effective Channel length (L_{eff}): The length of the channel estimated by the metallurgical junction for abrupt junctions

(3) Device width (w): The width of the device.

(4) Top gate thickness (t_{oxf}): The thickness of the front gate oxide.

(5) Buried oxide thickness (t_{oxb}): The thickness of the buried oxide.

(6) Silicon film thickness (t_s): The thickness of the silicon film

(7) Substrate thickness(t_{sub}):thickness of the substrate

(8) Applied potential (V_{gf} *and* V_{gb}): Potential applied at the front and back gates respectively.

(9) $N_B(x)$= Non uniform doping concentration in p-type SOI film

The 3-D Poisson's equation in the FD SOI film region with non uniform doping profile is given by[1]**,**

$$\frac{\partial^2\psi(x,y,z)}{\partial x^2}+\frac{\partial^2\psi(x,y,z)}{\partial y^2}+\frac{\partial^2\psi(x,y,z)}{\partial z^2}=\frac{q(N_B(x,y,z)-n(x,y,z)+p(x,y,z)+\Delta n}{\varepsilon_s} \quad (1)$$

where $\psi(x,y,z)$ is the surface potential at a particular point (x,y,z) in the SOI film, $N_B(x,y,z)$ is the non-uniform channel doping concentration , n(x,y,z) is the electron concentration, p(x,y,z) is the hole concentration , ε_s is the permittivity of silicon and Δ_n is the excess carriers generated per unit volume due to the absorption of incident optical power density.

The electron concentration, n(x,y,z) is given by,

$$n(x,y,z)=n_i e^{(\psi(x,y,z)-\mu_f(y))/V_T} \quad (1a)$$

Where n_i is the intrinsic carrier concentration, V_T is the thermal voltage and μ_f is the non-equilibrium quasi-Fermi level referenced to the Fermi level in the source that satisfies the following boundary conditions.

$$\mu_F(0)=0; \qquad \mu_F(L)=V_{ds} \quad (1b)$$

Where, L is the length of the channel and Vds is the drain to source voltage.

The non-uniform channel doping concentration $N_B(x,y,z)$ is given by [14],

$$N_B(x,y,z)=N_p \exp\left[-\left(\frac{x-R_p}{\sigma_p}\right)^2\right] \quad (2)$$

Where N_p is the peak concentration of the vertical Gaussian doping profile, R_p is the projected range and σ_p is the standard project deviation.

The depletion widths at the source and drain is given by[15]

$$y_S=\left[2\varepsilon_s\frac{(V_G+V_{bi})}{qN_B(x,y,z)}\right]^{1/2} \quad (3)$$

$$y_d = \left[2\varepsilon_s \frac{(V_G + V_D + V_{bi})}{qN_B(x,y,z)} \right]^{1/2} \quad (4)$$

Where, V_G and V_D are applied gate and drain voltages, ε_s is the permittivity of the semiconductor and V_{bi} is the built in potential.

The excess carriers generated per unit volume Δ_n , given by[16,17],

$$\Delta_n = \frac{1}{W_m} \int_0^{W_m} G_{op}(y)\tau_l dy \quad (5)$$

Where, W_m is the maximum width of the depletion layer and τ_l is the mean life time of minority carriers in the illuminated condition.

$$\tau_l = (n_i / (n_i + \Delta n))\tau \quad (6)$$

T being the life time of the carriers for the intrinsic semiconductor.

$$W_m = [4\varepsilon_s \ln(N_B / n_i) / q\beta N_B]^{\frac{1}{2}} \quad (7)$$

Where N_B is the non uniform doping concentration, n_i is the intrinsic carrier concentration, $\beta = \frac{q}{kT}$ k being the Boltzmann's constant, T is the absolute temperature.

$G_{op}(y)$ is the excess carrier generation rate at any point y in the semiconductor and is defined as,

$$G_{op}(y) = \frac{P_{opt}}{h\gamma}(1-R_m)(1-R_i)(1-R_s)\alpha e^{-\alpha y} \quad (8)$$

P_{opt} being the incident optical power density, and h is the Planck's constant , γ is the operating frequency and α is the absorption coefficient of the semiconductor at the operating wavelength. R_m,R_i and R_s are the reflection coefficient at the metal gate entrance, gate-insulator interface and insulator-semiconductor interface respectively.

The boundary conditions required to solve the 3-D Poisson's equation under illumination are [10],

$$\psi(0,y,z) - \frac{t_{oxf}}{\varepsilon_{ox}} \left[\varepsilon_{si} \left| \frac{\partial \psi(x,y,z)}{\partial x} \right|_{x=0} - Q_{it}{}^{f} \right] = V_{gf} - V_{fb}^{f} \quad (9)$$

$$\psi(t_s,y,z) - \frac{t_{oxb}}{\varepsilon_{ox}} \left[\varepsilon_{si} \left| \frac{\partial \psi(x,y,z)}{\partial x} \right|_{x=t_s} + Q_{it}{}^{b} \right] = V_{gb} - V_{fb}^{b} \quad (10)$$

$$\psi(x,0,z) = V_{bi} + V_{op} \quad (11)$$

$$\psi(x,L_{eff},z) = V_{bi} + V_{ds} + V_{op} \quad (12)$$

$$\psi(x,y,0) - \frac{t_{oxw}}{\varepsilon_{ox}} \left[\varepsilon_{si} \left| \frac{\partial \psi(x,y,z)}{\partial z} \right|_{z=0} - Q_{it}{}^{f} \right] = V_{gf} - V_{fb}^{f} \quad (13)$$

$$\psi(x,y,W) + \frac{t_{oxw}}{\varepsilon_{ox}} \left[\varepsilon_{si} \left| \frac{\partial \psi(x,y,z)}{\partial z} \right|_{z=W} + Q_{it}{}^{f} \right] = V_{gf} - V_{fb}^{f} \quad (14)$$

In eqns (9) and (10), V_{gf} and V_{gb} are the flat band voltages and Q_{it}^{f} and Q_{it}^{b} are the interface trapped charges associated with the front and back gates and ε_s and ε_{ox} are the permittivity for silicon and silicon dioxide respectively. In eqns (11) and (12), V_{bi} represents the built-in potential of the n^+ -p junctions and V_{ds} is the drain-to-source applied voltage, V_{op} is the photo induced voltage. Eqns (13) and (14) indicate that the potential applied at the front gate is the sum of the surface potential at the edge of the transistor and the drop across the sidewall oxide.

The 3-D effective mass Schrodinger equation in the space charge region of the device at drain end in the SOI MOSFET is given by

$$\frac{-\hbar^2}{2}\left(\frac{1}{m_x}\frac{d^2}{dx^2} + \frac{1}{m_y}\frac{d^2}{dy^2} + \frac{1}{m_z}\frac{d^2}{dz^2}\right)\psi(x,y,z) + qU(x,y,z)\psi(x,y,z) = E\psi(x,y,z) \quad (15)$$

where m_x*, m_y* and m_z* are effective masses in the x, y and z directions, respectively. m_x*=0.916m_0; m_y*=0.19m_0, and m_z*=0.19m_0. E is the eigen energy, $\hbar$ is the reduced Planck's constant, q is the charge of an electron, $U(x, y, z)$ is the surface potential, and ψ (x,y,z) is the eigen wave function.

The 3-D Schrodinger Eq. (8) is solved using the following boundary conditions.

$$\Psi_{y=0}=0 , \quad \Psi_{y=\text{Leff}}=1 ; \quad (16)$$

$$\Psi_{x=0}=0 , \quad \Psi_{x=\text{ts}}=0 ; \quad (17)$$

$$\Psi z_{=0}=0 , \quad \Psi_{z=\text{W}}=0 ; \quad (18)$$

3. Computational technique

The 3D Poisson's Eqn.(1) using the boundary conditions (9)–(14) is solved numerically using Leibman's iteration method to determine the surface potential for a fixed value of gate voltage and assumed value of drain voltage. This value of surface potential is then used in the 3D Schrodinger Eqn (15). The 3-D Schrodinger equation is then solved numerically using Leibman's iteration method and the exact value of surface potential is obtained. The potential at every point in the channel and its variation along the channel length is calculated using Leibman's iteration method as,

$$\psi(x,y,z)=\psi(x-1,y,z)+\psi(x+1,y,z)+\psi(x,y-1,z)+\psi(x,y+1,z)+ \\ \psi(x,y,z-1)+\psi(x,y,z+1)-(((qN_B(x,y,z)+p(x,y,z)-n(x,y,z))+\Delta_n)/\varepsilon_{si})/6) \quad (19)$$

An iterative approach has been adopted to calculate ψ (*x,y,z*) with the help of available boundary conditions. The potential at subsequent points towards drain end is calculated numerically and the device characteristics are estimated. We then implemented the 3D schrodinger wave equation with a finite difference grid with uniform spacing a. The derivatives appearing in the discrete Schrodinger equation are replaced with finite difference representations. The Schrodinger equation then reads,

$$-t_x(\psi_{i+1,j,k}+\psi_{i-1,j,k})-t_y(\psi_{i,j+1,k}+\psi_{i,j-1,k})-t_z(\psi_{i,j,k+1}+\psi_{i,j,k-1})+(V_{i,j,k}+2t_x+2t_y+2t_z)\psi_{i,j,k} \\ =E\psi_{i,j,k} \quad (20)$$

Where t_x,t_x, t_y, and t_z are the hopping energies given by,

$$t_x=\frac{\hbar^2}{2m_x^*a^2}\ ;\ t_y=\frac{\hbar^2}{2m_y^*a^2}\ ;\ t_z=\frac{\hbar^2}{2m_z^*a^2} \quad (21)$$

m_x*, m_y* and m_z* are effective masses in the *x*, *y* and *z* directions and '*a*' is the separation of grid line along *x, y, z* directions .

The field dependent Electric field is given by,

$$E_x=\frac{V(i+1,j,l)-V(i-1,j,l)}{\frac{2t_s}{a}} \quad (22)$$

$$E_y=\frac{V(i,j+1,l)-V(i,j-1,l)}{\frac{2L}{a}} \quad (23)$$

$$E_Z=\frac{V(i,j,l+1)-V(i,j,l-1)}{\frac{2w}{a}} \quad (24)$$

Where a is the separation of grid line along x, y, z directions ,*V(i,j,l)* is the surface potential and *L*, *W*, t_s are the gate length, device width & oxide thickness respectively.

The drain current I_{ds} including scattering effects is given by

$$I_{ds}=\mu w\frac{kT}{q}\frac{1-\exp(-qV_{ds}/k_BT)}{\int_0^{L_{eff}}\frac{dy}{\int_0^{t_s}qn_ie^{qU(x,y)/kT}dx}} \quad (25)$$

where *U(x,y)*is the surface potential, *k* is the Boltzman's constant and *T* is the absolute temperature,q is the charge of an electron.

The sub threshold swing S is a measure of the gate control on the channel. It can be expressed as,

$$S=\frac{\partial V_{gs}}{\partial\log I_{ds}} \quad (26)$$

The applied gate voltage V_{gs} and drain current I_{Ds} are related through the minimum of surface potential $U(x,y,z)_{min}$. Since the drain current at the subthreshold operation is dominated by diffusion process, the current may be computed in terms of the probability of source electron surmounting an energy barrier.The height of this barrier is $qU(x,y,z)_{min}$ where q is the charge of electron which is a function of applied gate voltage. Thus I_{ds} is proportional to exp($U(x,y,z)_{min}/V_T$) *where* V_T *is the thermal voltage.*

The photocurrent gain is given by ,

$$M=\frac{I_{ph}}{I_L} \quad (27)$$

where I_L is the primary current and is given by,

$$I_L=q\frac{P_{opt}}{h\gamma} \quad (28)$$

Responsivity R is defined as the output current divided by the incident light power

$$R=\frac{I_{ph}}{P_{opt}} \quad (29)$$

Quantum efficiency (η) is defined as the number of carriers generated per incident photon by a photodetector.

$$\eta=\frac{I_{ph}/q}{P_{opt}/h\gamma} \quad (30)$$

where I_{ph} is the photodetector current generated in response to incident light, q is the electron charge, P_{opt} is the incident optical power in watts, the quantity $h\gamma$ is the energy per photon in joules, where *h* is Planck's constant and γ is frequency.

Algorithm:

Step 1. Assign gate length, channel length, device width and gate oxide thickness of SOI MOSFET.

Step 2. Apply suitable bias voltages.

Step 3. Determine numerically the surface potential by solving the 3D Poisson's equation using Leibmann's iteration method by dividing the x, y and z axes each into 20 grids.

Step 4. Substitute this surface potential value in the 3D Schrodinger's equation.

Step 6. Solve the 3-D Schrodinger's equation .

Step 7. Calculate new n(x, y, z) value from the obtained wave functions and their corresponding eigen energies.

Step 8. A new surface potential value V(x, y, z) is obtained.

Step 9. Calculate the relative error of the surface potential between the exact and simulated values.

Step 10. Repeat step 4 to step 9 until it converges (Accuracy constant 0.0001) by increasing the number of iterations.

Step 11. Estimate the exact value of surface potential at every point along the channel length.

Step 12. Obtain electric field profile, drain and transfer characteristics and sub threshold swing of the device.

4. Results and discussion

Numerical computation has been carried out for the nano scale SOI MOSFET. The parameters used for the calculation are given in Table 1.The programs were written using 'visual c++' language and the diagrams were plotted using matlab.

Table 1.

Parameter	Value
Channel Length, L_{eff}	60nm
Gate Length, L_g	60 nm
Device Width, w	30nm
Buried oxide thickness, t_{oxb}	80 nm
Gate oxide thickness, t_{oxf}	1.2 nm
SOI film thickness ,t_s	15nm
Peak concentration,N_p	$1*10^{18}$ /cm^{-3}
Intrinsic carrier concentration,n_i	$9.65*10^{19}$/cm^{-3}
Plank constant, h	6.626×10^{-34} J-S
Temperature,T	300k
Mass of electron, m	9.109×10^{-31}C
Gate voltage, V_{gs}	0.7 V
Thermal Voltage,V_T	0.02582V
Critical field E_c	$1.65*10^6$ V/m
Low field mobility, μ_0	$0.2m^2$/V
Flatband voltage (V_{fb})	−0.48 V
Built-in potential (V_{bi})	0.6 V
Minority carrier life-time	10^{-3} s
Reflection coefficient at the metal gate entrance, R_m	10% of P_{opt}
Reflection coefficient at the insulator semiconductor interface, R_s	10% of P_{opt}
Reflection coefficient at the gate insulator interface, R_i	10% of P_{opt}
Projected range, R_P	1.5nm
Incident optical power, P_{opt}	0.5 W/ m^2
Absorption coefficient(α)	10^6/m

The potential distribution for dark and illuminated conditions in three dimensional SOI MOSFET with non-uniform doped channel is shown in Fig.3. It is seen that while the channel voltage remains same at the source and drain end of the gate in both dark and illuminated condition and the surface potential under illuminated condition is comparatively higher than that of dark condition. This can be very well explained with the help of Eqn. (1).

As seen from the equation, when more number of photo generated carriers is produced due to illumination, Δ_n increases which therefore increase the surface potential. The increase in potential is due to the photogenerated carriers and the external photovoltaic effects increase the conductivity of the channel in the illuminated condition.

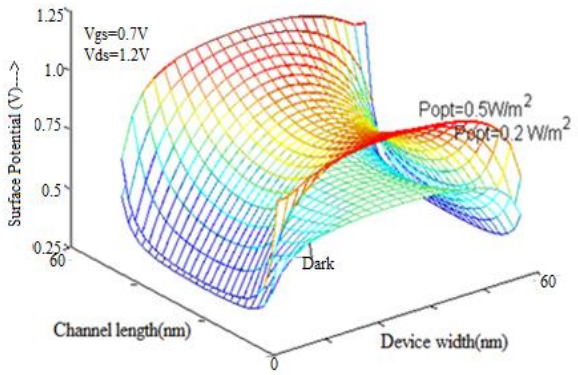

Fig. 3. Variation of surface potential for non-uniformly doped channel.

Fig.4 shows the variation of surface potential of SOI MOSFET photodetector for different values of projected range R_P and straggle σ_p . The optical power used for illuminating the device is P_{opt} = 0.5 W/m^2 and V_{ds} = 0.7 V. It is found that as the projected range increases, the surface potential along the channel length also increases for fixed values of straggle σ_p.

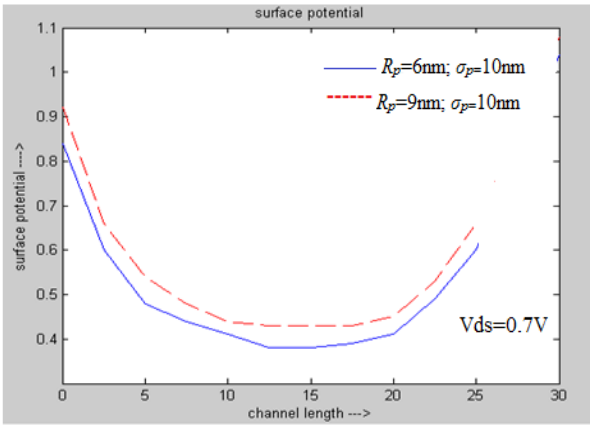

Fig. 4. Surface Potential variation along the channel length.

The variation of electric field with respect to channel length under dark and illuminated conditions is shown in Fig. 5. As seen from equations 22,23 and 24 electric field is directly proportional to potential. The electric field along the channel length increases due to quantum mechanical effects. The electric field increases slowly near the source end and rapidly near the drain end because the carrier density near the drain end experiences a rapid decrease in surface concentration which calls for a rapid increase in the electric field to maintain a constant drain current. It is seen that the electric field near the drain end in the illuminated condition is less compared to that in the dark condition needing a high drain voltage to attain saturation in the illuminated condition. When the device gets illuminated, more and more electron hole pairs are generated and more crowded.

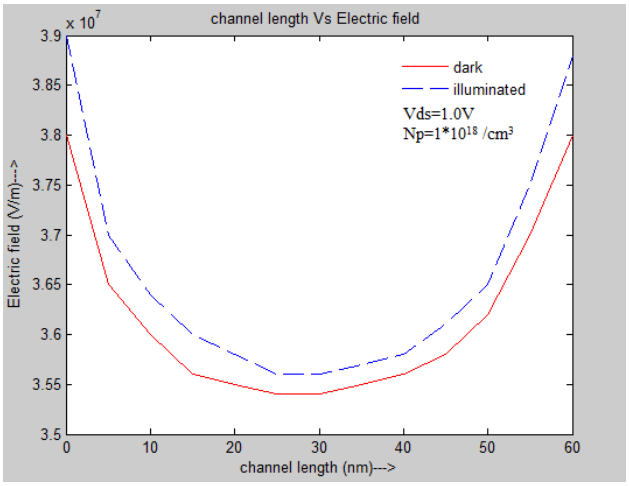

Fig. 5. Variation of Electric field under dark and illuminated conditions.

The variation of the drain current for different drain voltages is depicted in Fig. 6 for the dark and illuminated conditions. It is seen that the drain current increases significantly with the increase in drain voltage. The channel width is mainly determined by applied gate to source voltage. The charge carriers pass through the channel and thereby conduction is said to take place. When drain voltage increases further, more charge carriers try to pass through the channel due to which drain current increases. But the charge carriers can utilize only the channel width that is created earlier. That is the reason the drain current saturates after a certain limit even if drain voltage is increased further. The current under illuminated condition is higher and this is due to the generation of excess photo generated carriers under illumination.

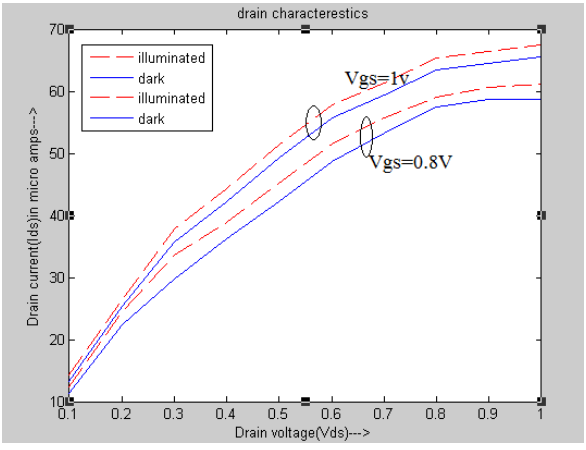

Fig. 6. Variation of Drain current under dark and illuminated conditions.

Fig. 7 shows the subthreshold swing for nanoscale SOI MOSFET. It is seen that Sub Threshold swing ‘s’ reduces with increasing channel length. It is also found that the subthreshold swing is slightly greater than that of dark condition.

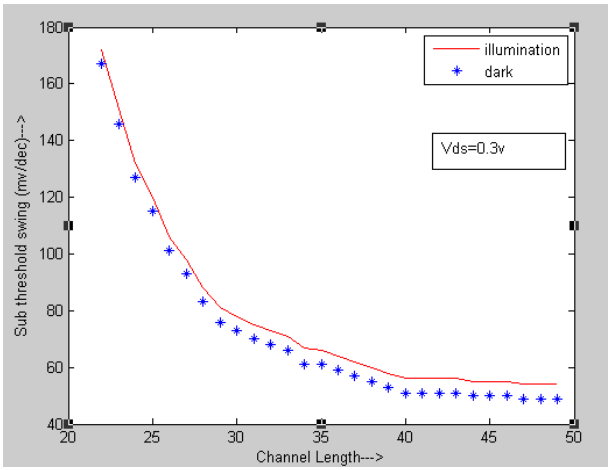

Fig. 7. Sub Threshold Swing along the length of the channel under dark and illuminated conditions.

The variation of the drain current for with respect to applied gate voltage is depicted in Fig. 8 for the dark and illuminated conditions. It is seen that the drain current decreases significantly with the increase in gate voltage. As the applied gate to source voltage increases, the drain current also increases for fixed drain voltage. This is due to the fact that the excess carriers generated in the channel. When the drain voltage increases, the drain current also increases rapidly.

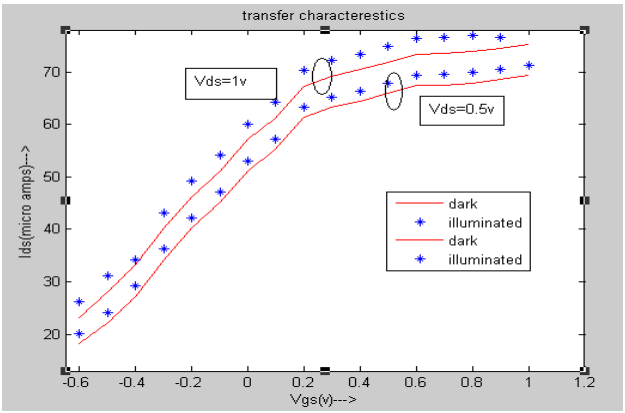

Fig. 8. Variation of Gate current under dark and illuminated conditions.

The effect of illumination on the current is shown in Fig. 9. It is also seen that the current increases as the V_{gs} values are increased. Due to the longer carrier lifetime, the photocurrent gets increased which increases the photoconductive gain as well as responsivity.

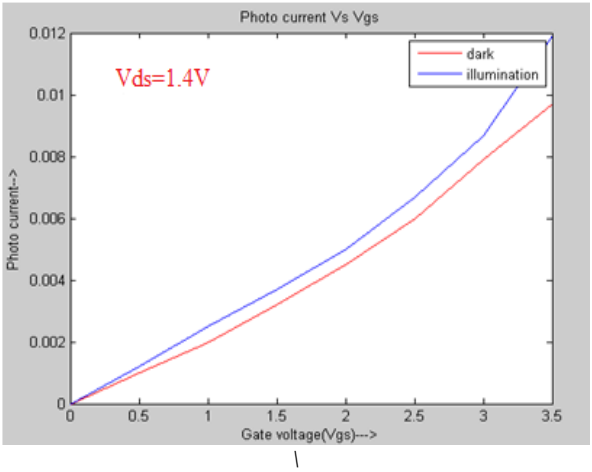

Fig. 9. Photo current Vs Gate voltage.

The variation of quantum efficiency with operating wavelength for fixed gare and drain voltages is shown in Fig. 10. It is seen that quantum efficiency is higher at lower values of wavelength. This is due to the minority carrier lifetime which limits the generation of the excess carriers.

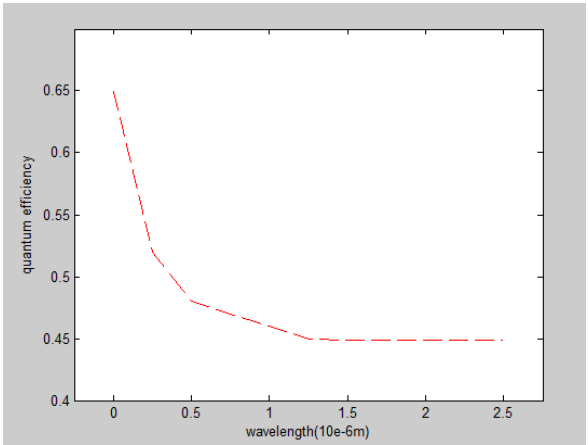

Fig. 10. Variation of quantum efficiency with operating wavelength.

Table 2. Parameters for SOI MESFET at V_{gs}= 0.3v, V_{ds}=0.4v.

Parameter	**Values**			
	Uniform Doping		**Non uniform Doping**	
Popt(W/m^2)	**0**	**0.5**	**0**	**0.5**
g_m (m mho)	252	379	52	79
C_{gs} (10^{-14} F)	24	35	14.8	32.5
r_d (k Ω)	7.6	4.8	9.74	6.24
RC timeconst (10^{-9}s)	5.62	3.19	6.12	4.63
Responsivity(m A/W)	---	0.534	---	0.132
Gain(dB)	---	96	---	97

The various parameters calculated for uniformly doped SOI MOSFET is compared with non-uniformly doped profile in Table 2. It is seen that the device has all the qualities required by a photodetector in OEIC receivers.

5. Conclusion

The 3D numerical modeling and simulation of nanoscale SOI MOSFET photodetector with non-uniform channel doping considering quantum mechanical effects is presented. The characteristics of the nanoscale SOI MOSFET photodetector shows that it may retain performance acceptable for OEIC receiver applications even if the gate length is reduced to nanoscale level. Accurate results have been obtained using Liebman's iteration method. In the future work, the detailed analysis of noise characteristics can be obtained, and equivalent circuit model could be developed for accurate characteristics of the device.

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*Corresponding author: aitecgowri@rediffmail.com; er.arun80@gmail.com