Performance analysis of pentacene-based OTFTs for high-speed circuit applications

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The aim of this article is to analyse the performance of an organic thin film transistor (OTFT) for high-speed circuits. As such, a simulation of the device with several insulators and different geometric parameters was conducted via Silvaco-TCAD. To assess the real performance of the device, we modelled the interface charge traps associated with the structural disorder of HfO_2 using a continuous trap density of states. I_{on}/I_{off} current ratio of $6.4x10^8$ and a switching frequency of 2.2 MHz were obtained in the optimal structure using HfO_2. The results suggest that the present OTFT, has potential applications in high-speed digital circuits.

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Keywords: OTFT, Electrical characteristics, Pentacene, Silvaco-TCAD, Switching frequency, Continuous trap density, Structural disorder

1. Introduction

Organic electronics is a recent field of scientific research that focuses on the applications of organic semiconductors in electronic devices [1-5]. Organic semiconductors are conjugated polymers composed of molecular chains based on carbon atoms linked with alternately single and double bonds. Charge transport in these materials is governed by p-bonding molecular orbitals [6]. The weak intermolecular interaction, of the van der Waals type, gives a flexible character to the molecular structure [7, 8]. This characteristic is unique to organic materials. Another important aspect is that the low processing temperature and cost-effective manufacturing of organic materials provide a foundation for future technological advancements [3, 9]. The multiple uses of organic devices, such as organic thin film transistors (OTFTs), solar cells, and organic light emitting diodes (OLEDs), in the fields of electronics and optoelectronics, serve as a further motivation for present and future intensive research activities. Indeed, OTFTs represent potential candidates for many applications in the field of electronics such as large-area flexible displays, portable electronics, bio-optical sensors, mobile device displays, smart televisions, and smart cards [10-14].

Although OTFTs have diverse uses, they deal with the challenge of relatively high operating voltages owing to the low carrier mobility of organic semiconductors [5]. This has encouraged considerable interest in optimizing device geometry, material engineering, characterization, and simulation to enhance performance OTFTs. Various structures have been proposed for manufacturing OTFTs, each exhibiting its unique benefits and disadvantages. However, the device structure is not the only factor determining device properties. The performance of OTFTs is also greatly influenced by the characteristics of the active layer and the gate insulator, which can be divided into two types: organic and inorganic [3]. Organic gate insulators, like poly(vinyl-phenol), PVP, poly(vinyl alcohol), PVA, and polyvinyl chloride, PVC, conduct to high operating voltages owing to their low dielectric permittivity. Whereas, inorganic materials namely Al_2O_3, HfO_2, and Ta_2O_5 are used to decrease operating voltage, but they may increase leakage current. Therefore, a detailed study of the dielectric materials is necessary for optimizing OTFT performance [15-17]. For this investigation, pentacene is adopted as the active semiconductor material. Its physical properties have been extensively characterised and widely reported in the literature, allowing pentacene to stand as a standard reference for TCAD modelling studies [1, 3, 4].

It remains a suitable candidate even though newer organic semiconductors, such as DNTT and its derivatives, are emerging in recent studies and can achieve higher field-effect mobilities [18].

In this article, we investigate the electrical properties of p-type pentacene-based OTFT with a bottom gate coplanar contact configuration. The DC characteristics of the device are simulated via Silvaco-TCAD considering several gate dielectric materials, such as SiO_2, Si_3N_4, Al_2O_3, and HfO_2. OTFT parameters (including on-state and off-state of currents and resistances) are analysed in relation to the dielectric constant, κ (also called relative permittivity, ε_r), active layer thickness, dielectric gate thickness, and channel length. Moreover, performance criteria, notably the on-off ratio and switching frequency of the present OTFT as a

switch, are determined under optimal conditions of the structure and analysed to identify the geometric factors that improve its characteristics.

Furthermore, as emphasized in extensive studies, structural disorder in amorphous metal oxides is an intrinsic source of charge traps, in addition to native defects [19, 20]. With this objective, we modelled these defects using a continuous trap density of states, specifically a Gaussian distribution, at the interface channel/gate dielectric. The quantification of the interface traps effects is analysed in the structure with HfO_2 as the gate insulator including the optimal geometric parameters.

2. Methodology

2.1. Simulation procedure

The simulation technique is carried out via Silvaco-TCAD (Technical Computer Aided Design). Simulation procedure is a sequence of several steps, which can be divided into three major parts: structure design, physical models including material parameters, and polarization conditions.

The designed structure of a typical pentacene-based OTFT is schematically illustrated in Fig. 1. This configuration, consisting of successive thin layers, is a bottom gate coplanar contact, where the gate is positioned at the bottom of the device whereas, drain and source electrodes are deposited at the same plane as the active layer which is pentacene. Geometric parameters of the present structure are listed in Table 1.

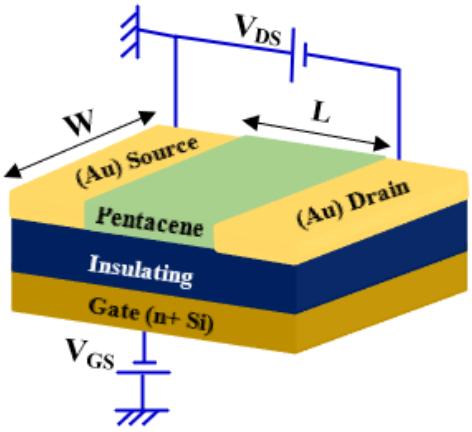

Fig. 1. Schematic diagram of the simulated structure of a pentacene-based OTFT (colour online)

Table 1. Geometric parameters of the designed structure

Parameters, (symbol)	Value [μm]
Pentacene thickness, (T_{osc})	0.02− 0.05
Channel length, (L)	2−10
Structure width, (W)	200
Substrate thickness	0.1
Insulating material thickness, (T_{ins})	0.1 − 0.4
Thickness of source/drain electrodes	0.02−0.05

Fig. 2 shows a flowchart illustrating the design phases for the simulated structure. The initial stage in the procedure consists of identifying the starting material, which is a phosphor-doped silicon substrate used as the gate electrode. A layer of an insulating material is then deposited, followed by a thin layer of pentacene that forms the active layer. After a step of etching to control the channel length, a gold layer is deposited on the same plane as the organic semiconductor. The design of the transistor is completed by an etching step which determines the drain and source electrodes of the transistor.

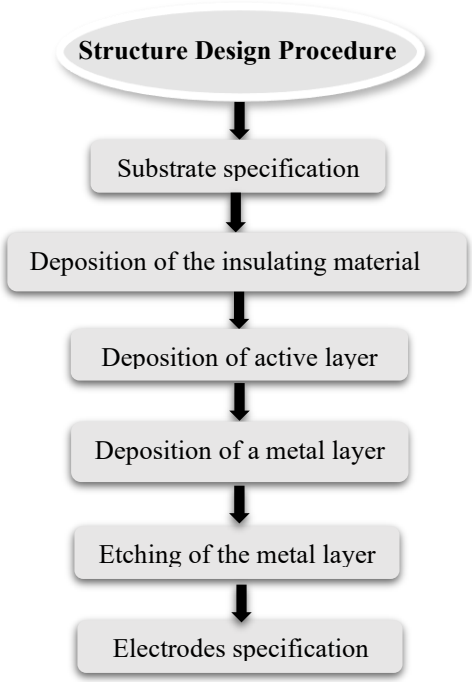

Fig. 2. Flowchart of an OTFT structure design via Silvaco-TCAD

In Silvaco software an electrode in contact with semiconductor material is assumed by default to be ohmic. If a work function is defined, the electrode is treated as a Schottky contact. The software calculates the surface potential (Ψ_S) at these interfaces using a self-consistent electrostatic model [21]:

$$\Psi_S = \chi + \frac{E_g}{2q} + \frac{K_B T}{q} \ln\left(\frac{N_C}{N_V}\right) - W_F + V_{APP} \qquad (1)$$

where χ is the electron affinity, Eg is the bandgap, K_B is the Boltzmann constant, T is the temperature, Nc and Nv are the effective densities of states in the conduction and valence bands and V_{APP} is the bias at the electrode. Furthermore, the Schottky barrier ϕ_B is determined using the following equation [21]:

$$W_F = \chi + \phi_B \qquad (2)$$

In our simulation, the source and drain electrodes are defined as Schottky contacts by specifying the work function of Gold (W_F = 5.1 eV) [1, 16], while the gate contact has a work function of 3.9 eV for heavily doped silicon. The choice of the gate metal affects the operating voltage, which decreases with a higher work function [10]. Additionally, the metal used for the drain and source electrodes determines the type of carriers injected into the channel.

It is important to note that in organic semiconductors, the HOMO (Highest Occupied Molecular Orbital) and LUMO (Lowest Unoccupied Molecular Orbital) levels are analogous to the valence band and conduction band, respectively, known in inorganic materials. Consequently, for an operating p-channel, the metal work function of the source, should be close to the HOMO level to allow holes injection when a negative voltage V_{DS} is applied, as shown in Fig. 3.

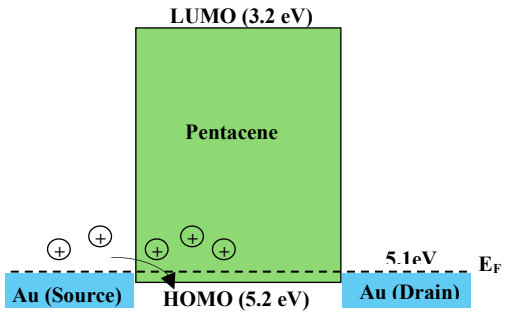

Fig.3. Energy band diagram of source drain electrodes in contact with pentacene [4] (colour online)

Furthermore, material characteristics of each layer, particularly the active layer are specified including parameters such as doping (P), bandgap (Eg), charge carrier mobility for holes and electrons (μ_{p0}, μ_{n0}) at zero field, relative permittivity (ε_r), electron affinity and effective density of states in both the conduction and valence bands (Nc, Nv) as shown in Table 2.

Table 2. Parameters of the active layer

Parameter	Value	Reference
P	3×10^{17} cm^{-3}	[22]
χ	2.8 eV	[13]
Eg	2.25 eV	[23]
ε_r	4.0	[16]
Nc	10^{21} cm^{-3}	[16]
Nv	10^{21} cm^{-3}	[16]
μ_{p0}	0.54 cm^2/Vs	[23]
μ_{n0}	7×10^{-4} cm^2/Vs	[23]

2.2. Physical models

Silvaco-TCAD employs fundamental physical models applicable to semiconductors simulations, including the Poisson equation and charge transport equations, while also integrating models for organic semiconductors transport mechanisms, solved using the finite element method to derive the device characteristics.

Molecular structure of most organic semiconductors is very disordered, and molecules are not chemically bonded to each other, resulting in a significant density of defect states and traps localized in the bandgap [7, 13]. Thus, the distribution of density of states in the bandgap is one of the most determining factors of transport mechanism and OTFTs characteristics. Gaussian distribution is often adopted for the trap density of states at deep levels, while an exponential variation in energy is chosen for the distribution of trap density of states at shallow levels [16, 24].

In the present simulation, we considered that total defect density of states consists of four constituents. Two constituents follow an exponential function $g_{TA}(E)$ and $g_{TD}(E)$ which are the acceptor-like and donor-like band tail function, respectively. The other two elements of the density of states, g_{GA} (E) and g_{GD} (E) follow a Gaussian distribution. The equations that describe these terms are given as functions of the trap energy E, the conduction band energy E_C, and the valence band energy E_V [16, 21, 24].

$$g_{TA}(E) = N_{TA}\exp\left[\frac{(E-E_C)}{W_{TA}}\right] \tag{3}$$

$$g_{TD}(E) = N_{TD}\exp\left[\frac{(E_V-E)}{W_{TD}}\right] \tag{4}$$

$$g_{GA}(E) = N_{GA}\exp\left[-\left[\frac{E_{GA}-E}{W_{GA}}\right]^2\right] \tag{5}$$

$$g_{GD}(E) = N_{GD}\exp\left[-\left[\frac{E-E_{GD}}{W_{GD}}\right]^2\right] \tag{6}$$

Table 3 summarizes the characteristics of defects at both shallow and deep levels, as well as the values employed in this simulation.

Table 3. Parameters characterizing defects at both shallow and deep levels

Parameter	Value	Reference
N_{TA}	2×10^{18} cm^{-3}eV^{-1}	[22]
N_{TD}	10^{18} cm^{-3}eV^{-1}	[22]
N_{GD}	6.5×10^{16} cm^{-3}eV^{-1}	[25]
N_{GA}	7×10^{16} cm^{-3}eV^{-1}	[26]
W_{TA}	0.1 eV	[22]
W_{TD}	0.5 eV	[23]
E_{GA}	0.62 eV	[22]
E_{GD}	0.78 eV	[22]
W_{GA}	0.15 eV	[22]
W_{GD}	0.15 eV	[22]

To explain these distributions in the bandgap, a plot of the density of states is given in Fig. 4, which shows the distribution of the shallow traps and that of the deep levels.

Organic semiconductors possess a low mobility due to their disordered structures and large defect concentrations, despite the increase in mobility with temperature. Thus, the models of band charge transport are inappropriate. Consequently, charge transport is explained through a hopping mechanism between localized states in both space and energy [7, 11].

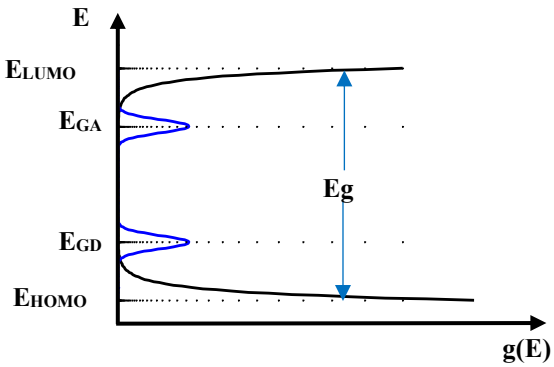

Fig. 4. Plot of the density of states distribution in the bandgap; Exponential distribution of shallow traps (black colour), Gaussian distribution of deep levels (blue colour) (colour online)

Particularly, Poole-Frenkel behaviour, observed in various conjugated polymers, is chosen into the Atlas simulation program. Based on this model, the electric field facilitates the delocalization of trapped charge carriers [17], leading to an increase in mobility that follows an exponential law, as expressed in the following equation [24].

$$\mu_{PF}(E) = \mu_{p0}\exp\left[-\frac{\Delta}{K_B T} + \left(\frac{\beta}{K_B T} - \gamma\right)\sqrt{E_x}\right] \qquad (7)$$

where μ_{p0} is the zero-field mobility (when drain voltage is zero [16]). E_x is the electric field parallel to the channel direction, Δ is the zero-field activation thermal energy (1.792×10^{-2} eV), β represents the Poole-Frenkel factor (7.758×10^{-5} eV $(cm/V)^{1/2}$) and γ is a fitting parameter [16, 23, 24].

3. Electrical characterization

3.1. Output and transfer characteristics

The calculated results of various investigated dielectric materials (SiO_2, Si_3N_4, Al_2O_3 and HfO_2) are represented in Fig. 5. The output characteristics plotted in terms of drain-source current (I_{DS}) versus drain-source voltage (V_{DS}) varying from – 20 to 0 V and at a constant gate-source voltage, V_{GS} = – 5 V are shown in Fig. 5 (a). Whereas, Fig. 5 (b) illustrates the transfer characteristics curves, i.e., I_{DS}-V_{GS} plots, obtained at V_{DS} = – 5 V with V_{GS} ranging from – 20 V to 0 V.

It can be seen that the drain-source current increases with increasing the dielectric constant: κ = 3.9 for SiO_2, κ = 7.5 for Si_3N_4, κ = 9.5 for Al_2O_3, and κ = 22 for HfO_2. For example, at $V_{GS} = V_{DS}$ = – 5 V, a drain-source current of 67.6 µA is obtained with HfO_2 structure which is about six times higher than that obtained with SiO_2 structure (I_{DS} = 9.7 µA).

Consequently, these results clearly put in evidence the influence of the gate insulator on the electrical characteristics of this simulated device. Since the simulated OTFT have a p-type active layer, drain current is technically negative. Hence, we refer to the absolute value to prevent any confusion regarding the direction of the currents.

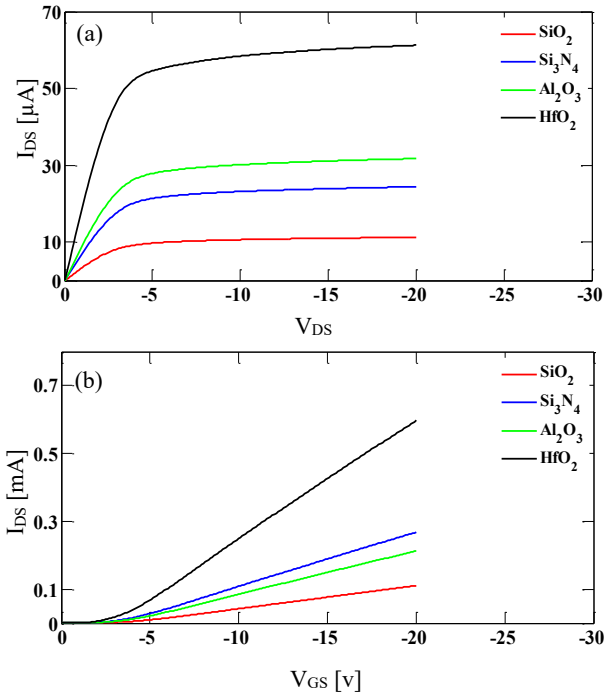

Fig. 5. Electrical characteristics of a pentacene-based OTFT with different gate dielectric materials: (a) output characteristics and (b) Transfer characteristics (colour online)

OTFT performance namely: the threshold voltage (V_{Th}), field effect mobility (μ_{FE}), transconductance (g_m) and subthreshold -swing (SS) values, are determined from the transfer characteristics for each insulating material and summarized in the table 4. It is important to note that in TCAD, V_{Th}, SS and g_m are directly extracted using integrated commands in TCAD tools. Field-effect mobility μ_{FE} is extracted from the transfer characteristic using the following formula [15]:

$$\mu_{FE} = \frac{I_{DS}}{C_i(V_{GS}-V_{Th})^2}\frac{2L}{W} \qquad (8)$$

Table 4. OTFT performance parameters for the considered insulating materials

Electrical parameter	SiO_2	Si_3N_4	Al_2O_3	HfO_2
V_{Th} [V]	-1.32	-0.98	-0.91	-0.73
μ_{FE} [cm^2/ V.s]	0.34	0.37	0.38	0.39
SS [V/dec]	0.21	0.15	0.13	0.097
g_m [μA/V]	6.93	13	16.3	33.1

It should be mentioned that μ_{FE} values ranging from 0.34 to 0.39 cm^2/V.s, are less than the input zero-field mobility parameter of 0.5 cm^2/V.s. This difference is primarily attributed to the coexistence of different transport mechanism within the organic semiconducting film. By implementing Coulombic trapping model in our simulation, the effective mobility is determined by Matthiessen's rule [21, 24]:

$$\frac{1}{\mu_{FE}} = \frac{1}{\mu_{PF}} + \frac{1}{\mu_{CB}} \tag{9}$$

where μ_{PE} represents the poole-Frenkel hopping mobility, and μ_{CB} incorporates the Coulombic scattering induced by the ionized trap states. Interestingly, a slight improvement of the effective mobility was observed with the use of high-k dielectrics, especially HfO2. This can be attributed to the increase in carrier concentration due to the increase in the gate capacitance.

3.2. ON- and OFF-state characteristics

The threshold voltage (V_{Th}) is an important parameter for the determination of the bias voltage needed for a transistor to operate in switching mode. In fact, a low V_{Th} value is advantageous since it allows switching at lower voltages. Based on the transistor threshold voltages ranging between – 0.73 and – 1.32 V, and saturation region being around V_{DS} = – 5 V, the following operating points are identified to characterize the on- and off-states.

On-state is defined by V_{DS} = – 5 V and V_{GS} = –5 V which is greater than the threshold voltage [27].

Off-state of the transistor is considered with V_{GS} = 0 V and V_{DS} = – 5 V. To characterize the on-state of an OTFT, two parameters are considered: the on-current (I_{on}) and the on-resistance (R_{on}). I_{on} is the drain current at V_{DS} = – 5 V and V_{GS} = – 5 V, R_{on} is the total resistance given by the following expression [4, 28]:

$$R_{on} = \left|\frac{\partial V_{DS}}{\partial I_{DS}}\right|_{V_{GS}=-5V} = R_{Ch} + R_C \tag{10}$$

where R_{Ch} is the intrinsic channel resistance and R_C is the contact resistance between the organic semiconductor and source/drain electrodes [4]. In the on-state, the transistor exhibits a relatively significant drain current I_{on}, associated with a low total resistance.

Fig. 6 illustrates the influence of the dielectric constant (ε_r) of the gate insulator on I_{on} (Fig. 6 (a)) and R_{on} (Fig. 6 (b)). It can be seen that increasing ε_r leads to an increase in I_{on} and a decrease in R_{on}. The highest I_{on} value of about 54.5 μA, with Ron ≈ 64 kΩ, is achieved with HfO_2 structure.

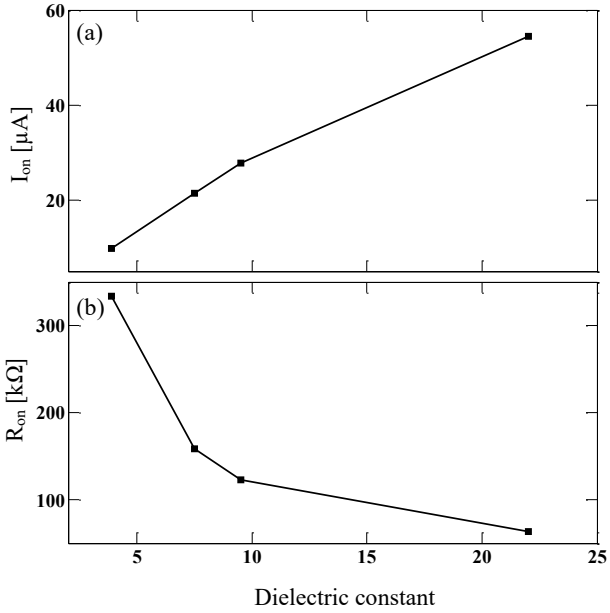

Fig. 6. Influence of dielectric constant on (a) on-state current and (b) on-state resistance

This behaviour, a significant effect of ε_r on I_{on}, is due to the accumulated charge carrier concentration at the interface: a higher dielectric constant enhances gate capacitance, which leads to more accumulated charges, and consequently to a higher current.

On the other hand, off-state of the transistor is characterized by the parameters off-current (I_{off}) when V_{GS} = 0 V and off-resistance (R_{off}). This low current is related to the channel conductivity (σ) and the voltage V_{DS} as well as geometric parameters: length (L), width (W) and the thickness of the organic semiconductor layer (T_{osc}); the expression of off-current is given by [30, 31]:

$$I_{off} = \frac{W}{L}\sigma V_{DS} T_{osc} \tag{11}$$

Off-state resistance (R_{off}) is defined as the ratio of the drain-source voltage (V_{DS}) to the off-state drain current (I_{off}). Without gate bias (V_{GS} = 0 V), the channel is only affected by the drain-source voltage V_{DS} enabling the determination of the equivalent resistance from the voltage-current ratio in the channel. Therefore, the relation of R_{off} can be expressed as [32]:

$$R_{off} = \frac{V_{DS}}{I_{off}} \tag{12}$$

An illustration of off-state current (I_{off}) and off-state resistance (R_{off}) as a function of the dielectric constant of the insulating material is represented in Figs. 7a and 7b, respectively.

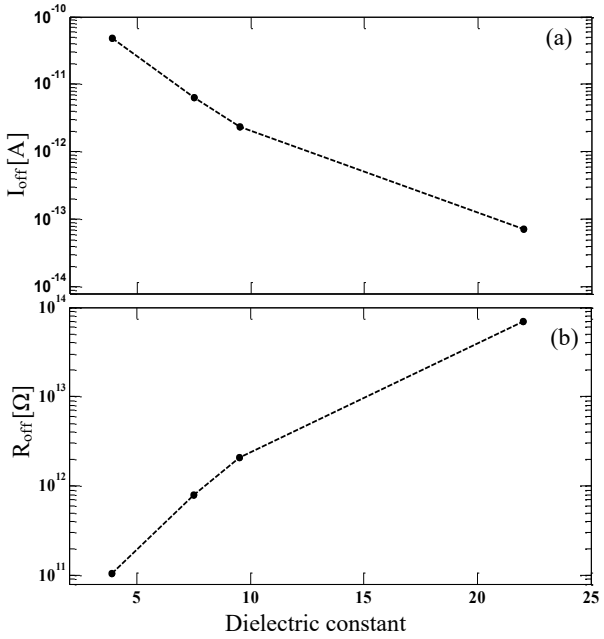

Fig. 7. Influence of dielectric constant on (a) off-state current and (b) off-state resistance

It is clearly seen that as the dielectric constant increases, I_{off} values considerably decrease from 81 pA for OTFT structure with SiO_2 to 0.07 pA for the OTFT structure with HfO_2. Whereas, R_{off} values increase from 10^{11} to ≈ $6x10^{13}$ Ω indicating an enhanced resistance to leakage currents. Therefore, these results emphasize that using high-κ dielectric materials can significantly enhance the isolation properties of transistors, contributing to better overall device performance.

4. Effects of geometric parameters

In order to determine the optimal configuration of the present OTFT, we investigate the dependence of the device characteristics on geometric parameters: the thickness of the insulating layer, the thickness of the active layer, and the channel length.

4.1. Insulating layers thickness

Fig. 8 illustrates the influence of thickness variations of insulating layers (SiO_2, Si_3N_4, Al_2O_3 and HfO_2) on the on-state parameters I_{on} (Fig. 8a) and R_{on} (Fig. 8b). It is clear that, for all materials, the current in the on-state increases as the insulating material thickness decreases. For example, when the thickness is reduced from 0.4 µm to 0.1 µm, I_{on} varies from 16.5 to 54.5 µA for HfO_2 and from 1.4 to 9.7 µA for SiO_2. However, the resistance in the on-state increases as the insulator thickness increases (Fig. 8 (b)) for all materials. The reciprocal behaviour of R_{on} to that of the on-state current is physically justified.

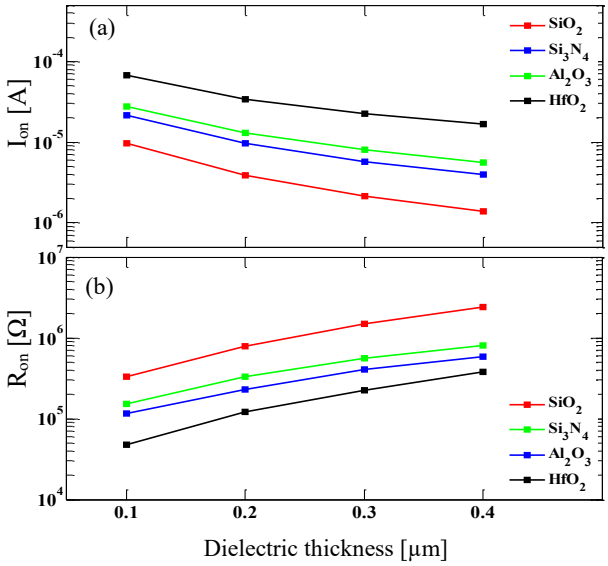

Fig. 8. Influence of dielectric thickness, for different gate dielectric materials, on (a) on-state current and (b) on-state resistance (colour online)

The magnitude of R_{on} for different insulating materials ranges from 0.04 to 0.3 MΩ, for the lowest thickness, in agreement with recent research on pentacene-based OTFTs [4]. This behaviour can be explained by the fact that the current flow in OTFT originates from the accumulated charge at the insulator-active layer interface. In fact, as the insulating layer thickness decreases, the capacitance for charge accumulation increases. Hence, the current flowing through the channel is improved. Consequently, the role of the insulating layer is crucial in keeping the transistor on by increasing charge storage within the channel.

It's crucial to note that Silvaco Atlas does not inherently simulate thin-film morphology or crystallinity. So, our simulations assume an optimized interface between the active layer and the dielectric. In practical devices, the high surface energy and roughness of untreated HfO_2 can hinder the growth of highly ordered organic crystals (e.g., edge-on stacking), potentially leading to a significant mobility degradation compared to SiO_2. Therefore, specific surface treatments, such as Self-Assembled Monolayers (SAMs), are required to ensure a smooth amorphous phase for achieving these theoretical findings practically [1].

Fig. 9 displays the variation of off-current and off-resistance as a function of the dielectric thickness for different insulating layers (SiO_2, Si_3N_4, Al_2O_3, and HfO_2).

It can be seen that, with decreasing the layers thickness, all the curves exhibit (i) a decrease of I_{off} and (ii) an increase of R_{off}. The minimum off-resistance value observed is 3.6 GΩ for the 0.4 µm oxide, while the maximum off-resistance value reaches 100 GΩ for the oxide. For HfO_2 R_{off} varies from 9.6×10^{10} to $6.8\ x10^{13}$ Ω.

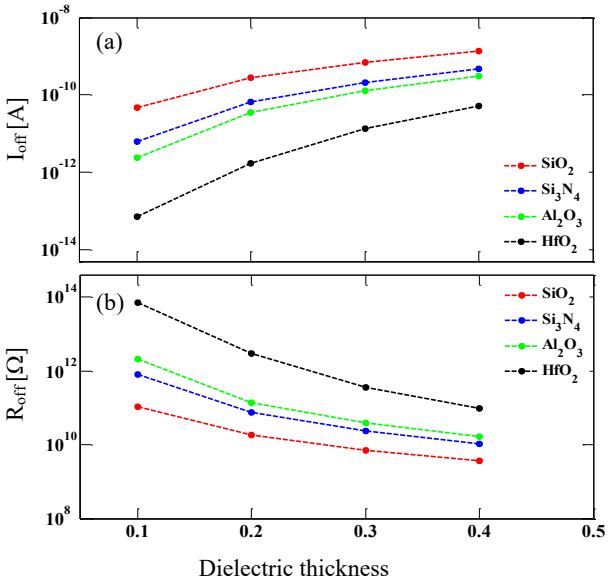

Fig. 9. Influence of dielectric thickness, for different gate dielectric materials, on (a) off-state current and (b) off-state resistance (colour online)

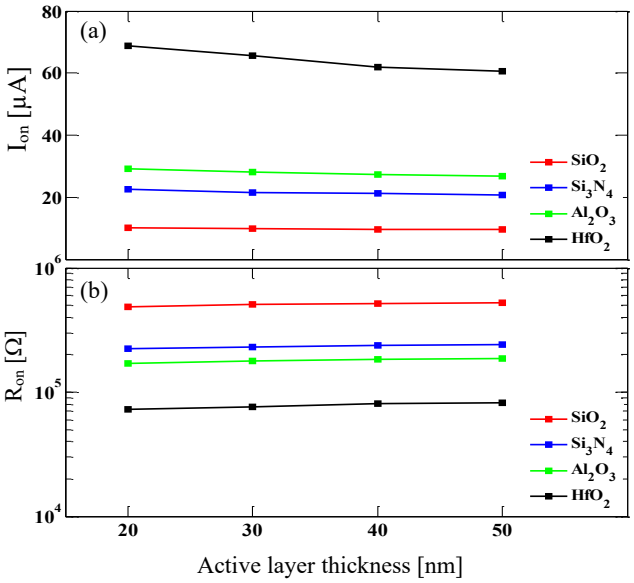

Fig. 10. Influence of active layer thickness, for different gate dielectric materials, on on-state (a) current and (b) resistance (colour online)

A reported variation of R_{off} between 0.01 and 1GΩ [22], are in the same order of magnitude range. A variation about 0.1 GΩ is also reported in reference [31]. The variation range of I_{off} is from 5.2×10^{-11} to 7.3×10^{-14} A for HfO_2, whereas for SiO_2, it ranges from 1.4×10^{-9} to 4.7×10^{-11} A as the insulating thickness decreases from 0.4 to 0.1 μm. In comparison to previous studies, an I_{off} current of approximately 3.28×10^{-9} A was reported in [33], while a lower I_{off} current within the same order of magnitude, was noted in [31]. Therefore, these results emphasize the important relation between insulating material thickness and performance criteria, indicating that the best performance of the OTFT is achieved with a thin insulating layer.

4.2. Active layer thickness

The active layer in a transistor is of great importance since it represents the origin of carriers and their pathway during the movement from the source to the drain [34, 35]. Hence, we study in this section the effects of the pentacene layer thickness on OTFT characteristics.

The simulation is performed with active layer thickness varied from 20 nm to 50 nm, while insulating layer thickness and channel length are maintained at 0.1 μm and 2 μm, respectively. The on-current and on-resistance versus active layer thickness for various gate-insulating materials are shown in Fig. 10a and 10b, respectively.

Interestingly, I_{on} remained rather stable despite variations in active layer thickness. This behaviour is related to the accumulation layer at the insulator-semiconductor interface. The accumulation layer, which is critical for current modulation, extends in the first monolayer near the interface and has a very thin thickness (~5 nm) [22, 25].

Despite the common idea that increasing the active layer thickness reduces channel resistance, the total resistance remains constant independent of pentacene thickness. This decrease is compensated by a rise in contact resistance, resulting in an overall constant total resistance as a function of the active layer thickness. The structure using HfO_2 has the lowest resistance (0.07 MΩ) and a maximum current of 68.7 μA with a pentacene layer thickness of 20 nm.

Fig. 11 illustrates the effects of the thickness of the pentacene layer (T_{osc}), for various gate-insulating materials, on I_{off} (Fig. 11 (a)) and R_{off} (Fig. 11 (b)). It is clear that, as the thickness of active layer decreases, the I_{off} current decreases for all dielectric materials; this behaviour is expected given that a thinner active layer results in an increased resistance as shown in Fig. 11 (b). Thus, I_{off} current variation is proportional to the thickness of the organic semiconductor layer, in agreement with relation (7) mentioned above [31].

Moreover, compared to previous studies conducted on OTFT with bottom gate top contact (BGTC) and bottom gate bottom contact (BGBC) configurations, the current in the on-state is mostly affected by the thickness of the active layer. The off-current, due to the bulk current, increases with increasing active layer thickness.

For instance, according to a recent study I_{off} increases from 3 to 39 nA when the thickness of the active layer ranges from 25 to 55 nm, [34, 35], which aligns with our results.

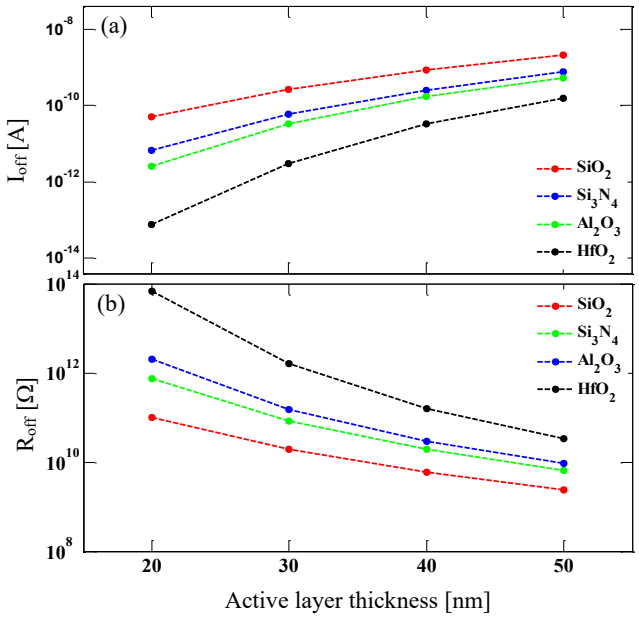

Fig.11. Influence of active layer thickness, for different gate dielectric materials, (a) off-state current and (b) off-state resistance (colour online)

Hence, lowering the pentacene layer thickness is necessary to reduce the off-current, which is usually required in display and memory circuits.

4.3. Channel length effects

To enrich this investigation, we consider the channel length which is another important parameter in OTFT design that controls the path of carriers between the drain and source electrodes. The effects of channel length variations from 2 to 10 µm on the on-state parameters are shown in Fig. 12a for I_{on} and in Fig. 12b for R_{on}.

The variations in OTFT characteristics for different channel lengths show that shorter channels induce a rise in on-current, and a reduction in on-resistance. For instance, when channel length decreases from 10 to 2 µm, I_{on} increases from 1.5 to 10.2 µA in the case of SiO_2 and from 10.2 to 68.7 µA for HfO_2. While R_{on} decreases from 1.8 to 0.3 MΩ for SiO_2 and from 0.3 to 0.04 MΩ for HfO_2.

These variations in I_{on} and R_{on} are in agreement with the literature [4]. The experimental values reported by W. Boukhili et al. [4] on pentacence OTFT with SiO_2 as a gate dielectric gives a total resistance in the order of 2×10^4 Ω at low V_{GS}, with a short channel (L = 2.5µm) and a value of 4×10^6 Ω for long-channel OTFTs (L = 10 µm) .

Recalling that the current in an OTFT is proportional to the W/L ratio. Hence, comparing the ratios W/L = 800 and W/L = 200/2 = 100 shows a strong agreement between the simulated values obtained in our case and the experimental values.

However, in short-channel OTFTs, contact resistance R_C at the source and drain electrodes becomes increasingly dominant leading to a non-linear voltage drop at the electrodes. To give a proportion of contact resistance R_C when the channel length is scaled down to 2 µm, we applied the following equations [14].

$$R_C = R_{tot} - R_{ch} \tag{13}$$

$$R_{ch} = \frac{L}{\mu_{po} C_i W (V_{GS} - V_{TH})} \tag{14}$$

The R_C/R_{tot} ratio is found to be 39.8% for the HfO_2 – based structure, while a higher proportion around 47% is obtained for the other insulating materials considered in our study.

Identifying that R_C accounts for nearly half of the total resistance reveals that the metal-semiconductor interface at the source-drain electrodes is a critical factor. This suggests that advanced contact engineering is required for further performance enhancements.

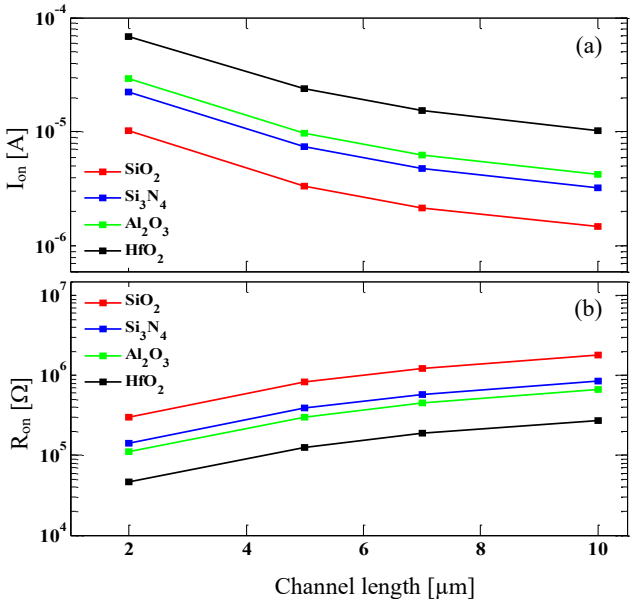

Fig. 12. Effects of channel length, for different gate dielectric materials, on (a) on-state current and (b) on-state resistance (colour online)

The off-state parameters dependence on channel length variations, in the range 2 to 10 µm, are plotted in Fig. 13 (a) for I_{off} and in Fig. 13 (b) for R_{off} for the considered dielectric materials. As can be seen, the channel length decrease leads to an increase in I_{off} and a decrease in R_{off}. The off-state current varies from 0.01 pA to 0.07 pA with HfO_2 and from 7.5 pA to 49.5 pA with SiO_2. These variations are accompanied by a decrease in R_{off} from 4.8×10^{14} Ω to 6.6×10^{13} Ω in the case of HfO_2 and from 6.6×10^{11} Ω to 1.0×10^{11} Ω with SiO_2.

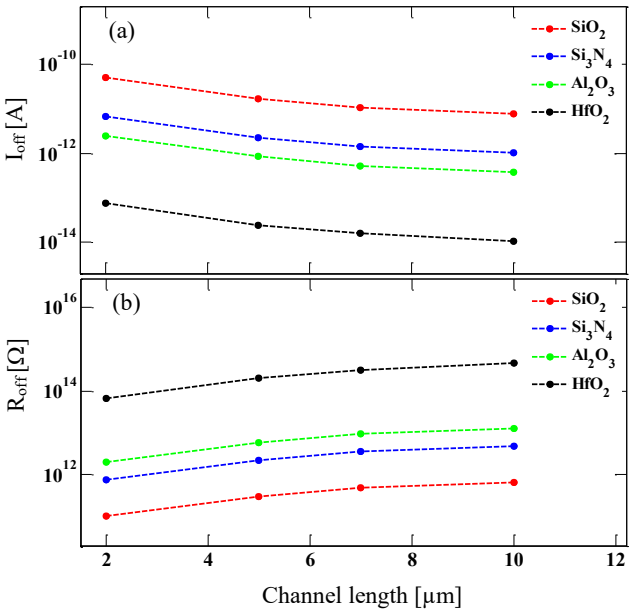

Fig. 13. Effects of channel length, for different gate dielectric materials, (a) off-state current and (b) off-state resistance (colour online)

In terms of the order of magnitude for off-resistance, we suggest a variation range between 100 MΩ to 550 MΩ for different polarization voltages as specified in the study of A. Arnal et al [32]. This range serves as an example for comparison with our results, indicating that the values are higher than those reported in their work. The observed behaviour is understandable because, in the off-state, the transistor is regarded as a resistance, which is directly proportional to channel length. Accordingly, a reduction in channel length leads to a decrease in R_{off} and an increase in I_{off}. Despite the variation of I_{off} and R_{off} with the reduction of channel length, the overall rise in these parameters remains low in OTFTs utilizing high-k dielectrics.

Nevertheless, the results demonstrate the substantial impact of channel length variation on OTFT operation in both on and off-states. A shorter channel length specifically causes an increase in both on- and off-currents.

5. Switching performance

Switching performance of organic thin-film transistors is a key factor for digital applications; it is critically dependent on two crucial parameters: the I_{on}/I_{off} current ratio and the switching frequency, f_S.

5.1. I_{on}/I_{off} current ratio

The current ratio, I_{on}/I_{off}, is defined as the ratio of drain-source current in the on-state to the current in the off-state as given by the following formula [3]:

$$\frac{I_{on}}{I_{off}} = \frac{I_{DS}|_{V_{GS}=-5V}}{I_{DS}|_{V_{GS}=0V}} \tag{15}$$

In this investigation, we consider the optimal pentacene-based OTFT characteristics determined above: (i) insulating layer thickness = 0.1 μm, (ii) active layer thickness = 0.02 μm, and (iii) channel length = 2 μm. Fig.14 (a) illustrates the variation of I_{on}/I_{off} ratio and f_S as a function of the dielectric constant under optimized conditions and at V_{DS} = - 5 V. A positive correlation is noticed between the I_{on}/I_{off} ratio and the dielectric constant.

As depicted in Fig. 14 a, the highest current ratio, approximately 7.5×10^8 is achieved with HfO_2 compared to 2×10^5 for SiO_2. These I_{on}/I_{off} ratio values are consistent with those reported previously for pentacene-based OTFTs, ranging from 10^4 to 10^8 [1, 9].

It is worth noting that, for switching applications, such as memories and displays, a high current ratio exceeding 10^6 is always desirable [9]. This indicates a good distinction between the two states and more effective suppression of leakage currents in the off-state. Therefore, the established values are suitable for digital electronics applications.

5.2. Switching frequency

The switching frequency of a transistor indicates the speed at which it can be turned on and off, as given by the following formula [29]:

$$f_S = \frac{1}{\tau_{rise}+\tau_{fall}} \tag{16}$$

where τ_{rise} and τ_{fall} are the switching rise time and fall time, respectively. It is the time required by the transistor to switch from the off-state to the on-state and vice versa. This time is associated with the charge and discharge time of the gate capacitance and is expressed as a function of the on resistance (R_{on}) and the gate capacitance (C_G) by the relation [28]:

$$f_S = \frac{1}{2\pi R_{on} C_G} \tag{17}$$

This formula is used to calculate the swithing frequency of the presently simulated pentacene-based OTFT. To explore the order of magnitude of the switching frequency, a curve of f_S versus the dielectric constant is plotted in the Fig. 14 (b). As the relative permittivity of the gate insulating material increases, the switching frequency values also increase. Switching frequency ranges from 3.45 MHz obtained with SiO_2 to 4.88 MHz achieved with HfO_2. Relative permittivity of insulating material is directly correlated with the gate capacitance responsible for the accumulation of the charge at the channel interface. With high-κ dielectrics (or high permittivity), the accumulated charge at the interface is high; consequently, the channel resistance as well as the total resistance of the device decreases. In fact, the charging time ($R_{on}C_G$) of the gate capacitance is decreased leading to an increased switching frequency.

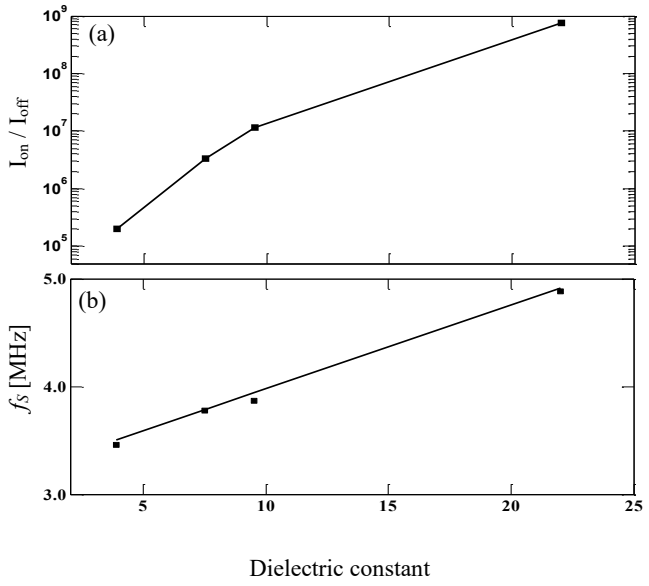

Fig. 14. Effects of dielectric constant (a) current ratio and (b) switching frequency

Therefore, these results emphasize the importance of high-k dielectrics to enhance the OTFT switching performance.

6. Modelling of interface trap states

The choice of HfO_2 as the gate dielectric allows for optimal theoretical performance due to its high dielectric permittivity. However, in practical manufacturing conditions, especially at low temperatures compatible with organic semiconductors, amorphous metal oxides such as HfO_2 exhibits a disordered structure [38]. This structural disorder is now recognized to be a primary source of electronic defects that act as intrinsic charge traps considerably affecting device performance [19, 20]. Therefore, a quantitative understanding of the impact of these traps is crucial to predict the real performance of devices.

Our model seeks to capture the physics of these traps by considering their origin, energetic distribution, and trapping kinetics at the dielectric/semiconductor interface.

6.1. Energetic distribution of traps

Oxygen vacancies (V_O) are commonly considered as the main defects in HfO_2. Experimental analyses have detected several discrete trap levels, which are attributed to these vacancies in monoclinic phase of HfO_2 [39].

However, it is established that the amorphous phase (a-HfO_2), even of high purity, contain a significant density of intrinsic charge traps arising directly from the disordered lattice, such as low-coordinated Hf ions and elongated Hf-O bonds [19]. These intrinsic defects create a broad continuum of deep states within the bandgap, acting as traps for electrons or holes [19]. The local structural variations within the disordered material generate a continuous distribution of intrinsic trap energy rather than discrete energy levels. This aligns with experimental observations and DFT calculations, revealing a wide band of deep traps in a-HfO_2 films, from 1.5 to 5.6 eV below the conduction band [20].

To capture this physical fact in our analysis, we examine an amorphous material with a disordered structure, which may exhibit defects such as oxygen vacancies [40]. Traps effect is particularly pronounced at the interface region between the dielectric and the active layer. Hence, we propose a model that represents the entire ensemble of interface traps—both oxygen vacancies and intrinsic disorder-related states—using a single Gaussian distribution, $g_{Dit}(E)$.

$$g_{Dit}(E) = N_{Dit} \exp\left[-\left[\frac{E-E_{git}}{W_{git}}\right]^2\right] \tag{18}$$

where N_{Dit} is the peak density of the distribution, E_{git} is its peak energy, and W_{git} represents the energy broadening induced by the disorder. Our analysis of the HfO_2/pentacene band alignment (Fig. 15) reveals that the experimentally observed deep traps in HfO_2 have energy levels located directly adjacent to the pentacene HOMO level.

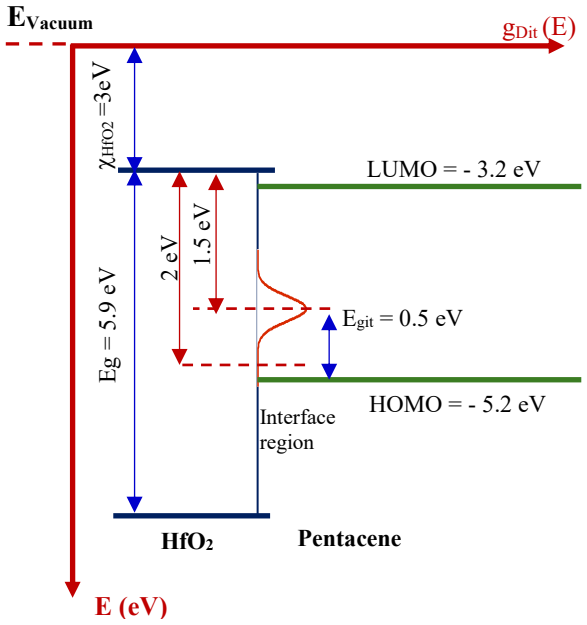

Fig. 15. Energy band diagram showing the Gaussian distribution of traps $g_{Dit}(E)$ at HfO_2/ pentacene interface (colour online)

The use of a Gaussian profile to encompass all interface traps (including oxygen vacancies and intrinsic disordered states) is fundamentally based on disorder theory [41]. Mathematically, the Central Limit Theorem dictates that the superposition of numerous independent random perturbations—including bond-length variations, atomic misplacements, and local electrostatic fluctuations—results

in a normal Gaussian distribution of energy states [42]. This statistical approach, serves as a reliable framework for describing charge transport in disordered materials dominated by localized state hopping. The unified Gaussian profile for the overall site energy distribution, which includes internal energy differences and polarization effects, has been confirmed by microscopic simulations [42].

Therefore, we have centred our trap energy distribution at 0.5 eV above the HOMO, for modelling a physically relevant class of defects positioned to capture holes from the channel.

6.2. Trap type and carrier capture kinetics

The amphoteric nature of defects in HfO_2 means their behaviour depends on the adjacent semiconductor. When interfaced with a p-type semiconductor like pentacene, these defects, intrinsic states and oxygen vacancies, act as efficient hole trapping centres [19, 39].

The trapping kinetics are defined by the capture cross-sections for electrons (σn) and holes (σp). While structural disorder and chemical vacancies in a-HfO_2 function as a unified kinetic system, we have adopted an approach that uses representative values based on experimental charge-trapping kinetics in a-HfO_2 MOS structures [43]. Accordingly, σn and σp were set to 3×10^{-13} cm² and 1.5×10^{-14} cm², respectively [43]. These parameters, considered as effective capture cross-sections, account for the multi-step trapping processes (tunnelling and hopping) facilitated by the disordered environment [43]. The use of a single cross-section value for the entire distribution is based on the assumption that all states within the distribution generate the same defect, which is an oxygen vacancy.

Recent research on the mechanism of defect generation in a-HfO_2 shows that carrier injection and charge trapping at intrinsic states (low-coordinated Hf ions and elongated Hf–O bonds) promote the formation of new defects, such as oxygen vacancies [40]. Electrons or holes localized at these trapping sites strongly reduce the activation energy for bond breakage of adjacent Hf–O bonds resulting in the creation of new oxygen vacancies leading to the degradation of the dielectric properties [40].

Therefore, we suggest that both pre-existing oxygen vacancies and the generated ones are the central defect type in both the initial and degraded states of HfO_2, and we consider single capture cross-sections as representative values for the entire trapping process.

6.3. Quantification of the impact of traps on OTFT performance

To quantify the effect of these defects, we simulated the output and the transfer characteristics for different interface densities of states (N_{Dit}), from 4×10^{11} to 2×10^{12} $cm^{-2}eV^{-1}$. Fig. 16 overlays the obtained I_{DS}-V_{DS} (Fig. 16 (a)) and I_{DS}-V_{GS} characteristics (Fig. 16 (b)).

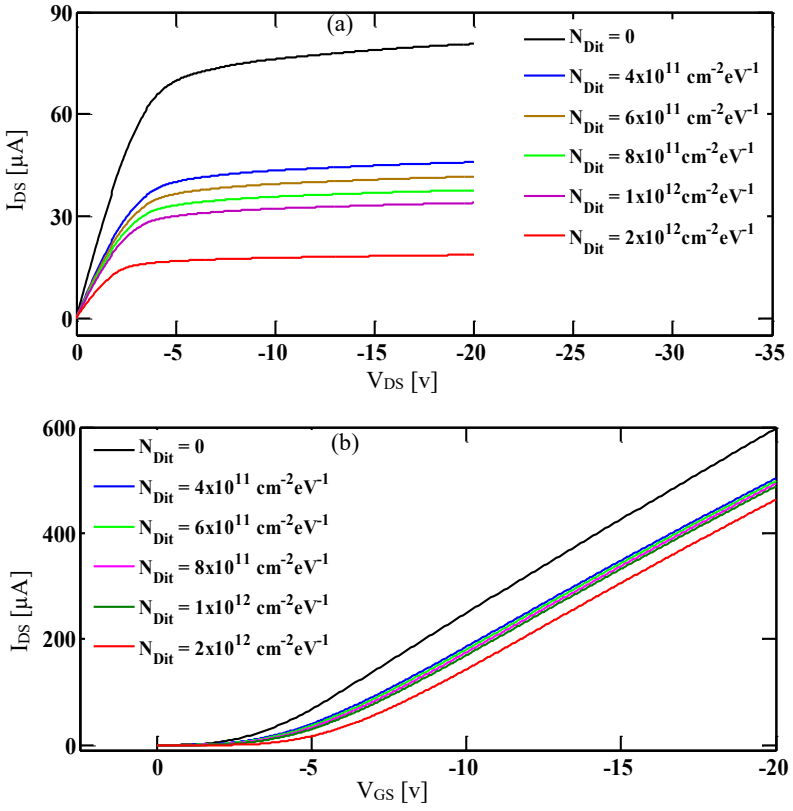

Fig. 16. Interface traps effects on (a) out-put characteristics (b) Transfer characteristics (colour online)

The extracted key parameters are summarized in Table 5, which illustrates the impact of interface trap density on the device performance.

Table. 5. Interface traps effect on OTFT performance

N_{Dit} [10^{11} cm^{-2} $.eV^{-1}$]	V_{Th} [V]	μ_{FE} [cm^2/ Vs]	SS [V/dec]	I_{on}/ I_{off} (10^8)	f_S [10^6 Hz]
0	-0.7	0.40	0.09	7.5	4.8
4	-1.8	0.27	0.12	6.6	2.6
6	-2.0	0.26	0.14	6.7	2.4
8	-2.2	0.26	0.15	6.6	2.3
10	-2.3	0.25	0.16	6.4	2.2
20	-3.1	0.19	0.22	4.5	1.4

Analysis of the results presented in Table 5 reveals a systematic variation of OTFT performance with increasing interface trap density. The most direct and pronounced consequence of increasing trap density is a shift in threshold voltage toward more negative values. A higher density of traps requires a higher voltage to achieve a conduction state, due to hole trapping, thus V_{Th} shifts from -1.8 V to -3.1V as the trap density increases from 4×10^{11} to 2×10^{12} cm^{-2} eV^{-1}. Channel conductivity decreases with the reduction of the density of charge carriers available in the channel leads to an increase in on- resistance and a decrease in on- current, which leads to a decrease in the I_{on}/I_{off} current ratio from 7.5×10^8 to 4.5×10^8. On the other hand, charge mobility is reduced thus affecting the transistor ability to transition from the off-state to the on-state. This effect is reflected in the increase in the subthreshold slope parameter (SS).

Due to the increased channel resistance, the switching speed of the transistor decreases resulting in a switching frequency that drops from 4.8 MHz to 1.4 MHz. Nevertheless, the order of magnitude of the current ratio and the switching frequency demonstrate the capacity to implement OTFTs in fast digital electronic circuits with a frequency around 1 MHz [1, 29].

In comparison to the experimental studies**,** a frequency of approximately 1 MHz was obtained for a pentacene-OTFT with a channel length of 1 µm, and the interface charge estimated to be 2.8×10^{11} cm^{-2} [28]. Our results reveal a switching frequency of 2.3 MHz with a total density of 4×10^{11} cm^{-2} and a channel length of 2 µm demonstrating a significant increase in performance. Experimental studies have shown the potential of operating a dual-gate OTFT-based circuit at a frequency of 50 kHz and a supply voltage of 10 V [37].

Table 6 shows the optimal performance compared to values reported in previous studies. The simulated results are obtained at a total trap density of 4×10^{11} cm^{-2}, which is close to the commonly estimated experimental value of 2.5×10^{11} cm^{-2} for short-channel pentacene OTFTs [4, 28].

Table 6. Comparison of optimal simulated results with previously reported values

Parameter	Present work	Reported values	Ref
V_{Th} [V]	-2.2	(-0.4)−(-8.5) (-2.5)− (-12.5)	[1] [32]
I_{on} [A]	33.2×10^{-6}	0.06×10^{-6} 1.5×10^{-6}	[1] [36]
R_{on} [Ω]	8×10^4	0.07×10^4– 25×10^4	[4]
I_{off} [A]	5×10^{-14}	10^{-14} – 3×10^{-12} 10^{-10}–10^{-9}	[31] [32]
R_{off} [Ω]	9×10^{13}	10^7 – 10^9 10^8–5.5×10^8	[44] [31]
I_{on}/I_{off}	6.6×10^8	7.9×10^8 10^6–10^{10}	[1] [15]
f_S [Hz]	2.3×10^6	0.5×10^6–1×10^6 0.05×10^6	[28] [37]

7. Conclusions

A pentacene-based organic thin film transistor with bottom gate and coplanar contact configuration was investigated via Silvaco software. Several dielectric materials (SiO_2, Si_3N_4, Al_2O_3 and HfO_2) were considered as well as different geometric parameters: the thicknesses of both insulating and active layers as well as the channel lengths. The analysis of output and transfer characteristics, using different gate insulating materials, put in evidence that the choice of the insulating material has a substantial impact on overall electrical characteristics of the device. Best values of electrical parameters namely on-current, off-current, on–resistance, off-resistance, I_{on}/I_{off} current ratio and switching frequency are achieved with HfO_2. Therefore, high-k dielectric materials are required in OTFT design due to the gate capacitance that accumulates charges in the conducting channel.

The analysis of geometric parameters effects revealed that both the insulating layer thickness and the channel length contribute to the multiplication of the I_{on} current. Whereas the thickness of the active layer does not significantly affect the I_{on} current, as the accumulation layer that generates the drain-source current forms in a very thin region close to the interface with the insulator.

Hence, to realize optimized pentacene-based OTFTs with a bottom-gate and coplanar contact configuration, it is recommended to use (i) HfO_2 dielectric layers of 0.1 µm in thickness, (ii) channels with 2 µm in length, and (iii) pentacene active layers of 20 nm. Regardless of interface traps effect, this structure shows promising potential for high-speed applications, with an I_{on}/I_{off} ratio of 7.5×10^8 and a switching frequency of 4.8 MHz.

Furthermore, our study demonstrated that the performance of this optimized structure is strongly influenced by the presence of charge traps at the HfO_2/pentacene interface. By modelling these defects with a realistic state distribution, we quantified their impact: a typical peak trap density of 1×10^{12} cm^{-2} eV^{-1}leads to a shift in the threshold voltage (from -0.7 V to -2.3 V), a reduction

in the switching frequency (from 4.8 MHz to 2.2 MHz) and a decrease of current ratio (from $7.5x10^8$ to $6.4x10^8$).

These findings emphasise that properly engineered pentacene-based OTFTs serve as a reliable foundation for high-speed electronic circuits. Furthermore, the physics-based simulation framework developed in this work is designed to be generically extensible. By adjusting specific molecular parameters—such as the Gaussian density of states and hopping transport coefficients—this model can be readily adapted to simulate the performance of other high-mobility, air-oxidation-resistant molecules (e.g., DNTT derivatives). Consequently, while this study focuses on pentacene as a benchmark, the results provide a solid basis for the optimisation and predictive design of a broader range of next-generation organic integrated systems.

Conflicts of interest

The authors declare that they have no conflicts of interest.

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