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Quantitative analysis of SOI memory cells

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A quantitative analysis for describing and discussing design characterization of a SOI (Silicon-on-Insulator) flash memory cell is presented. Expressions for the front gate threshold voltage of a SOI memory cell are derived using equations for the standard SOI MOSFET. Coupling coefficients connecting the control gate with the source and drain region, and with the silicon bulk via charge stored at the floating gate, have to be included in these equations. In this way, the front gate voltage of the standard SOI MOSFET is equal to the voltage of the memory cell floating gate. During analysis, emphasis is put on the case when the back channel is depleted, because in that case coupling between the front and back gate can control the threshold voltage of the control gate. The derived expressions show the influence of the back voltage V_{G2} and device parameters on the threshold voltage of either the control or floating gate, when the device is fully depleted.

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1. Introduction

Interest in Silicon-on-Insulator (SOI) devices has been motivated by its superiority over bulk silicon in radiation environment and by prospects for 3-dimensional integration [1]. A SOI device is very similar to a conventional bulk device except that a buried insulator, most commonly silicon dioxide, separates the active region of the device from the silicon substrate. Presence of a buried oxide results in several novel advantages of SOI in comparison to conventional bulk technologies. The device is fully insulated from the neighbouring components via the buried oxide and lateral insulation. This results in a significant decrease of parasitic capacitances and improves the speed performance of SOI circuits. In addition, the subthreshold slope is steeper and the leakage current smaller. The main advantage of SOI at low voltage and low power arises from the junction capacitance reduction [2]. Research of SOI devices has shown that they are very convenient for high density VLSI circuits [3,4].

2. Analysis of standard SOI MOSFET

Standard SOI transistor is shown in Fig. 1. It is a four terminal enhancement mode SOI n-channel MOSFET fabricated on an insulating layer of buried silicon-dioxide. Two different kinds of devices are currently investigated: partially depleted or "thick-film" devices and fully depleted or "thin-film" devices. SOI devices are fully depleted when the width of depletion regions is larger than the silicon film thickness. The threshold voltage varies with the back gate bias due to the coupling effect between the front and back gates, when the silicon film is fully depleted. If a large negative or positive bias is applied to the back gate, thin accumulation or inversion layers will be present at the back interface, respectively. However, fully depleted devices with depleted back interface exhibit some of the most favourable properties, such as low electric fields, high transconductance, excellent short channel behavior, and quasi-ideal subthreshold slope. The focus of analysis is on the threshold voltage of the cell, since it is one of the most important parameters of the design. Using depletion approximation, the Poisson equation becomes:

$$\frac{d^2\Psi}{dx^2} = \frac{qNa}{\varepsilon_{Si}} \qquad (1)$$

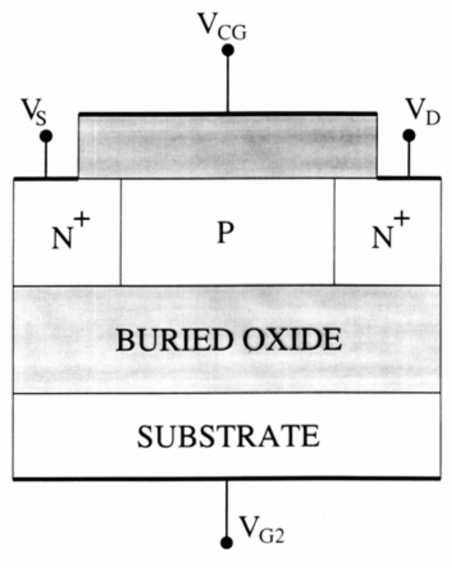

Fig. 1. SOI MOSFET.

where Na is the doping concentration of the silicon body. Equation (1) can be solved by double integration, yielding the potential as a function of depth in silicon film, x [2]:

$$\Psi(x) = \frac{qNa}{2\varepsilon_{Si}}x^2 + (\frac{\Psi_{S2} - \Psi_{S1}}{t_{Si}} - \frac{qNa\, t_{Si}}{2\varepsilon_{Si}}) + \Psi_{S1} \quad (2)$$

where Ψ_{S1} and Ψ_{S2} are the potentials at the front and back silicon-oxide surfaces, respectively, and t_{Si} is the thickness of silicon film.

Applying Gauss' theorem to the front and back Si-SiO_2 surface:

$$V_{G1} = \Phi_{MS1} + \frac{Q_{OX\,1}}{C_{OX\,1}} + \left(1 + \frac{C_{Si}}{C_{OX\,1}}\right)\Psi_{S1} - \frac{C_{Si}}{C_{OX\,1}}\Psi_{S2} - \frac{\frac{1}{2}Q_{depl} + Q_{INV\,1}}{C_{OX\,1}} \quad (3)$$

where V_{G1} is the front gate voltage, Φ_{MS1} is the difference between the work function Φ_M of the front gate and the silicon work function Φ_S, $Q_{OX\,1}$ is the fixed charge density at the front Si-SiO_2 interface, $C_{OX\,1} = \frac{\varepsilon_{OX}}{t_{OX\,1}}$ is the front gate oxide capacitance, $C_{si} = \frac{\varepsilon_{Si}}{t_{Si}}$ is the body capacitance, Q_{depl} is the depletion charge density and $Q_{depl} = -qNa\, t_{Si}$, where t_{Si} is the thickness of silicon film and Q_{INV1} is the front carrier charge density.

Similarly, $V_{G2} = \Phi_{MS2}$

$$\frac{Q_{OX\,2}}{C_{OX\,2}} - \frac{C_{Si}}{C_{OX\,2}}\Psi_{S1} + \left(1 + \frac{C_{Si}}{C_{OX\,2}}\right)\Psi_{S2} - \frac{\frac{1}{2}Q_{depl} + Q_{S2}}{C_{OX\,1}} \quad (4)$$

where V_{G2} is the back gate voltage, Φ_{MS2} is the back gate-body work function difference, $C_{OX\,2} = \frac{\varepsilon_{OX}}{t_{OX\,2}}$ and Q_{S2} is the charge in the back channel.

Combining equations (3) and (4) leads to the dependence of the front gate voltage on the back gate voltage. As we can see from these two equations, both voltages depend on the device coupling coefficients.

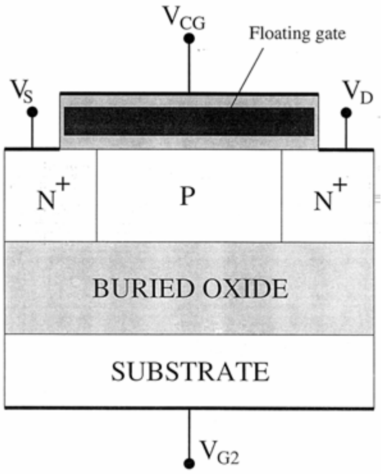

Fig. 2. SOI Flash memory cell.

There are 3 different possible steady-state charge conditions at the back interface:

a) the back surface is accumulated

b)

$$V_{G1} = \Phi_{MS1} - \frac{Q_{OX\,1}}{C_{OX\,1}} + \left(1 + \frac{C_{Si}}{C_{OX\,1}}\right)(V_S + 2\phi_B) - \frac{\frac{1}{2}Q_{depl}}{C_{OX\,1}} \quad (5)$$

where Ψ_{S2} is equal to zero and $\Psi_{S1} = V_S + 2\phi_B$, where $\phi_B = \frac{kT}{q}\ln\left(\frac{Na}{n_i}\right)$ is the Fermi potential of the silicon body; then $Q_{INV\,1}$ is equal to zero.

b) the back surface is inverted

$$V_{G1} = \Phi_{MS1} - \frac{Q_{OX\,1}}{C_{OX\,1}} + (V_S + 2\phi_B) - \frac{\frac{1}{2}Q_{depl}}{C_{OX\,1}} \quad (6)$$

where $\Psi_{S1} = \Psi_{S2} = V_S + 2\phi_B$.

c) the back surface is depleted

Ψ_{S2} is strongly dependent on V_{G2}; it's value ranges from zero to $2\phi_B$ between the onsets of accumulation and inversion, respectively. The values of V_{G2} varies between these onsets: $V_{G2,\,ACC} < V_{G2,\,depl} < V_{G2,\,INV}$. The value at the front surface is $\Psi_{S1} = 2\phi_B$ and $Q_{INV\,1} = Q_{S2} = 0$. Inserting these conditions into (4) and combining with (3) gives:

$$V_{G1} = V_{G1.\,ACC2} - \frac{C_{Si}C_{OX\,2}}{C_{OX\,1}(C_{Si} + C_{OX\,2})}(V_{G2} - V_{G2,\,ACC}) \quad (7)$$

$$= V_{G1.\,INV2} - \frac{C_{Si}C_{OX\,2}}{C_{OX\,1}(C_{Si} + C_{OX\,2})}(V_{G2} - V_{G2,\,INV}) \quad (8)$$

3. SOI flash memory cell

SOI Flash memory cell configuration is illustrated in Fig. 3. The flash memory cell is made with a dual layer of heavily-doped n^+ polysilicon gate. Dual-polysilicon layer of the memory cell gate makes the voltage applied to the control gate much higher than in case of a single polysilicon layer gate. Therefore, in order to turn the memory cell on, the applied voltage has to be at least equal to the sum of the floating gate threshold voltage and the voltage drop across the oxide between the control and floating gates [5,6,7]. In expressing the control gate threshold voltage we will use equations derived for the front gate threshold voltage of the standard SOI transistor, simply using voltage of the floating gate in the place of the front gate voltage. Fig. 3 shows the capacitive network of such a gate. The floating gate is capacitively coupled to the control gate, the drain, the source and the silicon surface.

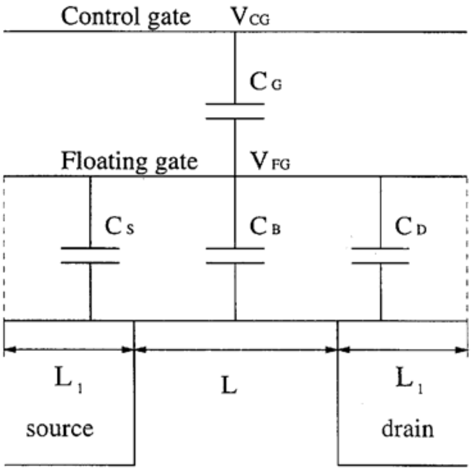

Fig. 3. Capacitive network of the floating gate

From the charge balance condition, charge on the floating gate Q_{FG} is given by [8]:

$$Q_{FG} = C_B (V_{FG} - \psi_{S1} - \phi_{MS1}) + C_G (V_{FG} - V_{CG}) + C_D (V_{FG} - V_D) + C_S (V_{FG} - V_S) \tag{9}$$

where V_{FG} is the floating gate voltage, ψ_{S1} is the silicon surface voltage of the floating gate in the channel region, ϕ_{MS1} is the difference between the work function ϕ_M of the floating gate and the silicon work function ϕ_S. C_B, C_G, C_D and C_S are the capacitances between the floating gate and the silicon body, the control gate, the drain and the source, respectively, as shown in Fig. 3. C_B, C_G, C_D and C_S are given as:

$$C_B = (\varepsilon_{OX} / t_{OX1})\, W\, L \tag{10}$$

$$C_G = (\varepsilon_{OX} / t_{OXG})\, W\, (L + 2L_1) \tag{11}$$

$$C_D = C_S = (\varepsilon_{OX} / t_{OX1})\, W\, L_1 \tag{12}$$

where ε_{OX} is the dielectric constant of S_iO_2, t_{OX1} is the oxide thickness between the floating gate and the silicon body, t_{OXG} is the oxide thickness between the floating gate and the control gate, W is the channel width, L is the channel length and L_1 is overlapping between the floating gate and source (drain) section. From equation (9) it follows:

$$V_{FG} = (1/C_T)\,[C_G V_{CG} + C_D V_D + C_S V_S + C_B (\psi_{S1} + \phi_{MS1}) + Q_{FG}] \tag{13}$$

where

$$C_T = C_G + C_D + C_S + C_B \tag{14}$$

Transistors characteristics of the structure shown in Fig. 2 should be those of a conventional SOI n-channel MOSFET, whose gate voltage is given by (13). Further, equation (13) provides a connection between the floating gate and the control gate, so combining (13) with (3) and (4), one can relate the threshold voltage of the control gate to the back gate voltage and device parameters. According to these equations, a detailed expressions of the control gate threshold voltage as a function of different possible steady-state charge conditions at the back interface is derived:

1) the back surface is accumulated

$$V_{TC,\,ACC2} = 1/C_G \{\phi_{MS\,1} (C_T - C_B) + (V_S + 2\varphi_B)\,[(1 + C_{Si}/C_B)\,C_T - C_B] - C_D V_D - (C_G + C_S)\,V_S - C_T (Q_{OX\,1}/C_{OX\,1} + Q_{depl}/2C_{OX\,1}) - Q_{FG}\} \tag{15}$$

2) the back surface is inverted

$$V_{TC,\,INV2} = 1/C_G \{(\phi_{MS\,1} + V_S + 2\varphi_B)(C_T - C_B) - C_D V_D - (C_G + C_S)\,V_S - C_T (Q_{OX1}/C_{OX1} + Q_{depl}/2C_{OX1}) - Q_{FG1}\} \tag{16}$$

3) the back surface is depleted

$$V_{TC,\,depl2} = V_{TC,\,ACC2} - C_T C_{Si} C_{OX2}\,[V_{G2} - V_{G2,\,ACC2}] / C_G C_{OX1} (C_{Si} + C_{OX2}) \tag{17}$$

$$= V_{TC,\,INV2} - C_T C_{Si} C_{OX2}\,[V_{G2} - V_{G2,\,INV2}] / C_G C_{OX\,1} (C_{Si} + C_{OX\,2}) \tag{18}$$

Derived equations are checked by inserting empirical results into them and comparing the obtained values of the front gate threshold voltage. Next we consider certain parameters of the cell design. Graphs are obtained using QUATTRO PRO, in the manner described above. It can be seen that as V_{G2} increases from $V_{G2,ACC}$ to $V_{G2,INV}$ [by $(2\varphi_B + V_S) + (1 + C_{Si}/C_{OX2})$], V_{TC} decreases linearly with V_{G2} from $V_{TC,ACC}$ to $V_{TC,INV}$ [by decrease of $(2\varphi_B + V_S)\, C_T C_{Si} / C_G C_{OX1}$)]. The surface potential corresponding to inversion and accumulation differs from zero and $(2\varphi_B + V_S)$, respectively, by a few thermal voltages (nkT/q, $n \sim 5$ [9]) depending on the degree of inversion and accumulation. Usually, V_{G2} is fixed or changing rapidly.

4. The silicon film thickness

The silicon film thickness t_{Si} is an important parameter of a thin-film fully depleted SOI MOSFET. Indeed, t_{Si} influences all electrical parameters of a thin film (threshold voltage, subthreshold slope etc.). Dependence of the control gate threshold voltage V_{TC} of a fully depleted cell on silicon body thickness t_{Si} is shown in Fig. 4. It can be seen that for accumulated back channel V_{TC} decreases as t_{Si} increases. Such behaviour is expected, because when the back channel is accumulated t_{Si} is smaller, the electric field at the back interface is sufficiently high and of the same direction as the electric field at the front interface, so that a higher threshold voltage has to be applied. When the back channel is depleted (fixed V_{G2}, $V_{G2,INV} < V_{G2} < V_{G2,ACC}$), V_{TC} increases with t_{Si}. This can be explained as follows: as t_{Si} increases for a fixed V_{G2}, depletion layer stays the same, until at a certain point the transistor is no longer fully depleted and V_{TC} is the same as for bulk. All the analysis described previously were performed with the condition that the silicon body is depleted, because only in that case does the charge coupling between the front and back gates exist. From [9] the maximum depletion region width extending from an inverted interface is:

$$x_{D\,MAX} = [2\varepsilon_{Si}(2\varphi_B)/qN_a]^{1/2} \qquad (19)$$

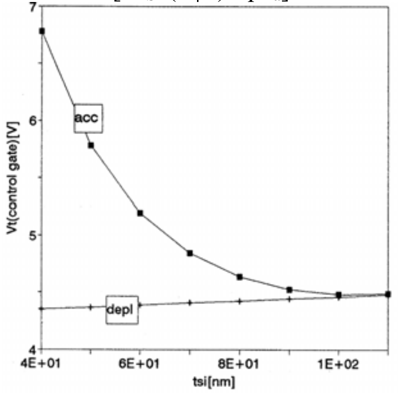

Fig. 4. Threshold voltage of control gate V_{TC} versus t_{Si}

This means that the above equations are valid for $t_{Si} \le x_{D\,MAX}$. If $t_{Si} \ge x_{D\,MAX}$ then:

$$V_{TC} = 1/C_G\,[(C_T - C_G)(2\varphi_B + \Phi_{MS1}) - C_S(V_D - V_S) + C_T K(V_S + 2\varphi_B)^{1/2} - Q_{FG}] \qquad (20)$$

where $K = (2q\varepsilon_{Si}N_a / C_{OX1})^{1/2}$. If $x_{D\,MAX} \le t_{Si} \le 2x_{D\,MAX}$ then:

$$V_{G2,\,con} = \Phi_{MS2} + (1 + 1/C_{OX2})\,qN_a(t_{Si} - x_{D\,MAX})^2 / 2\varepsilon_{Si} + qN_a(t_{Si} - x_{D\,MAX})/2C_{OX2} \qquad (21)$$

where $t_{Si} - x_{D\,MAX}$ is the depletion region width at the back interface. For $V_{G2} \le V_{G2,\,con}$ the silicon body is not fully depleted and $V_{G2,\,threshold}$ is equal to (20). For $V_{G2} \ge V_{G2,\,con}$ the silicon body is fully depleted. For $V_{G2,con} \le V_{G2} \le V_{G2,INV}$, V_{TC} is the same as in equation (17) and for $V_{G2} \ge V_{G2,INV}$, V_{TC} is the same as in equation (16). Fig. 5 shows the dependence of V_{TC} on V_{G2} for several ratios of t_{Si} and $x_{D\,MAX}$, with $x_{D\,MAX}$ determined by N_a as described by equation (19). As expected, sensitivity of V_{TC} to V_{G2} diminishes as t_{Si} increases, because V_{TC} depends on V_{G2} for a fully depleted cell, as can be seen from the equations, so if t_{Si} increases and the same voltages are kept, the cell will not be fully depleted any more.

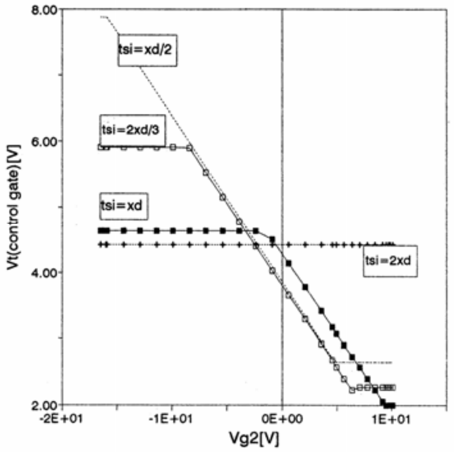

Fig. 5. Dependence of V_{TC} on V_{G2} for different t_{Si} and fixed $x_{D\,MAX}$.

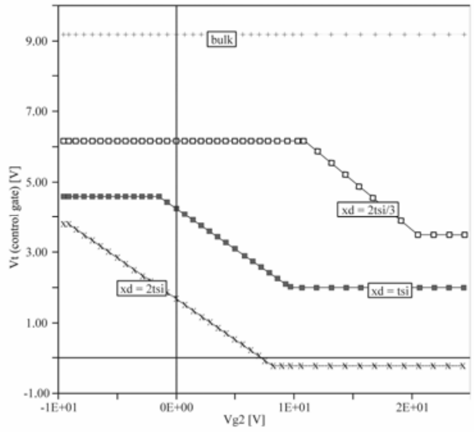

Fig. 6. Dependence of V_{TC} on N_a for different $x_{D\,MAX}$ and fixed t_{Si}

Fig. 6 shows the dependence of V_{TC} on the doping concentration N_a defined by equation (19), for different values of $x_{D\,MAX}$ and for a fixed thickness of the silicon film t_{Si}. This dependence is obtained by plotting V_{TC} versus V_{G2}. As can be seen, V_{TC} becomes less sensitive to N_a as V_{G2} decreases ($x_{D\,MAX}$ increases), and the sensitivity of V_{TC} to V_{G2} is enhanced until $x_{D\,MAX}$ reaches t_{Si}.

5. Conclusion

It is very important for a designer to predict how a certain device will behave when its parameters are changed. Specifically, when designing flash memory arrays it is necessary to know the write/erase window, e.g. the value of front gate threshold voltage for write/erase operations. Starting from the well-known equations for the front gate threshold voltage of a standard SOI MOSFET, we have derived equations for the front gate threshold voltage of a SOI memory cell. We have deduced a very important conclusion from the analysis, that a SOI memory cell can be considered similar to a standard SOI MOSFET, except that the charge stored at the floating gate during the write/erase cycle has to be taken into account. Once knowing the equations for the front gate threshold voltage, one can project other design parameters.

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