JOURNAL OF OPTOELECTRONICS AND ADVANCED MATERIALS Vol. 12, No. 12, December 2010, p. 2413 - 2418

Rectifying characteristics and equivalent circuit of the epitaxial n-PbTe/p-Si heterojunction

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In the present work, preparation of n-PbTe epitaxial layer was grown on p-Si single crystalline substrate by means of liquid phase epitaxy. The crystalline structure and morphology of n-PbTe/p-Si heterojunctions were characterized by X-ray diffraction (XRD) and scanning electron microscope (SEM). The results showed high quality PbTe thin films were directly deposited onto p-type silicon (111) substrates .The current-voltage characteristics were measured in the temperature range 300-400 K. The n-PbTe/p-Si heterojunctions showed a good rectification ratio at the bias voltage of ±1.5 V at 300K.The electronic parameters such as series resistance, ideality factor barrier height were determined. The two series RC components electrical model in order to study the dynamic behaviour of the Schottky diode in low frequency and to improve the effect of barrier inhomogeneities in electrical properties were used.

(Received October 29, 2010; accepted November 25, 2010)

Keywords: PbTe, Thin film, LPE, p-Si

1. Introduction

Lead chalcogenides, as PbS, PbSe and PbTe are narrow band gap semiconductors which have shown great promise in the field of IR photodetectors [1-4], thermophotovoltaic [4] and thermoelectric devices [5]. The unique properties of lead salt diode lasers are the wide wavelength operating range, high mobility, good thermoelectric properties, tunability, narrow line width, and high local and temporal resolution [6-7]. Other advantages of these materials are the good homogeneity, rather low price, and easier manufacturing relative to HgTe-based materials.

Semiconductor thin films could be deposited on silicon substrate, which is known to be the basic material for modern microelectronics. The growth of $A^{IV}B^{VI}$ thin films on Si substrates allows producing the monolithic structures for IR sensor arrays with the charge storage and signal multiplexing performed on the same chip [8].

Various techniques could be used for producing PbTe thin films on the monocrystalline Si such as molecular beam epitaxy (MBE)[9], chemical bath deposition[10], chemical vapor deposition[11], electrodeposition[12], vapor deposition[13] , and electrochemical atomic layer epitaxy (ECALE)[14] have been developed for the growth of lead chalcogenide semiconductors.

Epitaxial growth of PbTe films directly on the Si wafer is desirable for the simplification of the fabrication process. The direct growth of epitaxial PbTe on Si (1 1 1) by the HWE technique had been undertaken by Vaya et al.[15]

Epitaxial growth of PbTe directly also on Si to fabricate a PbTe/Si heterostructure on p-type Si (1 0 0) by hot-wall epitaxy (HWE) without an intermediate buffer layer, was studied by Yang et al. [16]. They have demonstrated the possibility to grow PbTe directly on Si (1 0 0) by hot wall epitaxy (HWE). They have grown a single crystal n-type PbTe overlayer on a p-type Si (1 0 0) substrate, and obtained a more efficient heterojunction detector can operate at room temperature. In the present work, we have demonstrated a high quality of PbTe thin film directly grown on Si (1 1 1) substrate by liquid phase epitaxy. We studied the temperature dependence of the current–voltage characteristics in both forward and reverse bias in an attempt to obtain information about the device parameters. In addition, the dynamic properties were studied by capacitance measurements and correlated to the properties of Schottky diode.

2. Experimental

2.1. Device preparation

The p-type Si (111) single crystalline wafers with carrier concentration of 10^{15} cm^{-3} is obtained from Nippon Mining Co. Pieces of 1 cm^2 each and 450 μm thick were cleaned and etched by using the CP4 solution ($HF:HNO_3:CH_3COOH$ in ratio 1:6:1). After etching, the Si wafers were washed with distilled water and then with ethyl alcohol just before the epitaxial deposition of PbTe layer.

The liquid phase epitaxy technique was employed to grow epilayer of n-PbTe on p-Si single crystal wafers using indium as a solvent. The multibin boat made of special graphite hardness is held in a fixed position within a silica tube, and a thermocouple is fixed under the boat. Prior to the growth process, purified argon is passed through the tube in order to get rid of any contamination. The LPE technique is described in detail elswhere [17].

The loaded boat was heated up to 750 K and kept at this temperature for 30 min to homogenize the solution and then cooled down with a cooling rate of 5 K/min. The growth process is terminated by removing the substrate with its upper epilayer from the solution cell. The schematic diagram of n-PbTe /p-Si heterojunction is shown in Fig.1.

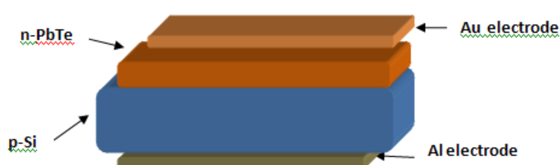

Fig.1 Schematic diagram of n-PbTe/p-Si heterojunction

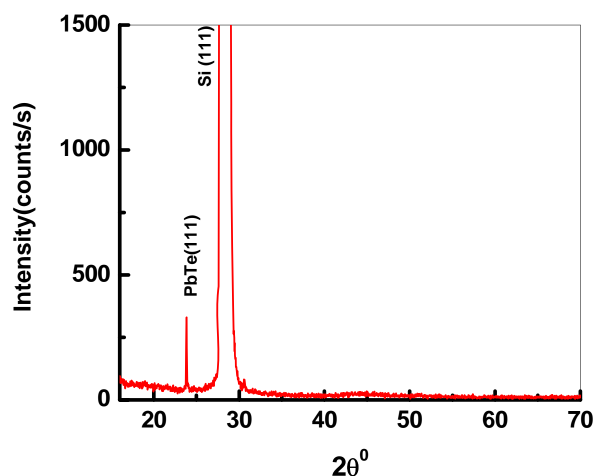

Fig. 2. X-ray diffraction patterns of n-PbTe /p-Si heterojunction..

2.2. Measurements

Scanning electron microscope model JEOL-5940 was used to study the surface morphology of the n-PbTe/p-Si heterojunctions.

X-ray diffraction (XRD) analysis was car using Philips X-ray diffractometer model X'pert filter and CuK$_\alpha$ radiation .

The current–voltage (*I–V*) measurement performed by the use of a high impedance Keith programmable constant current source electromet temperature range of 300–400 K. The temperat always monitored by using a copper–co thermocouple close to the sample. The capa voltage (*C–V*) characteristics were performed by th a 410 *C–V* meter at 1 MHz. For the *C–V* measu small sinusoidal signal of 30 mV peak to peak external pulse generator is applied to the sample to meet the requirements. All *C–V* measuremen carried out with the help of a computer through AC/DC converter card.

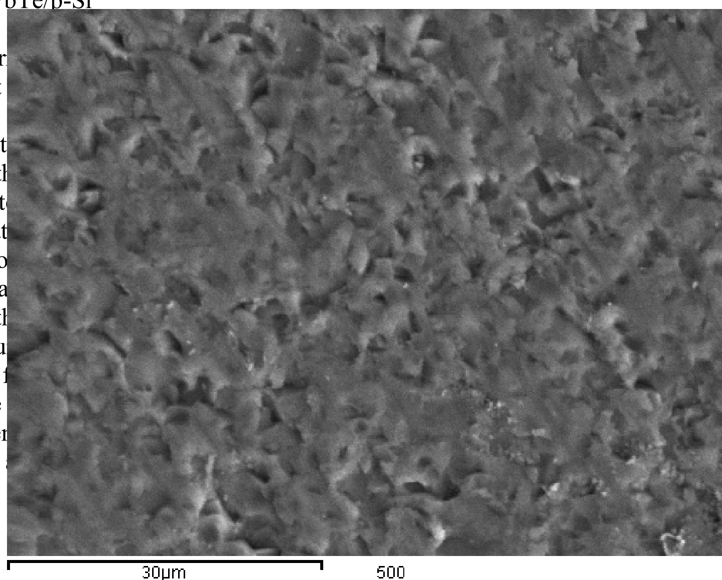

Fig.3. SEM micrograph of PbTe epilayer deposited on silicon substrate.

3. Results and discussion

3.1 Crystal structure and surface morphology

X-ray diffraction patterns, XRD of n-PbTe/p-Si heterojunction is shown in Fig. 2. Two discrete sharp peaks with low and high intensity are obsereved that confirming the monocrystalline structure for both PbTe and Si with the same (111) orientations, respectively. The peak positions and their relative intensities of PbTe films and Si substrate are consistent with those of a standard cubic structure according to 65-0470 and 89-5012 ICDD cards. It is clearly observed that the direct LPE yields a good PbTe film on single crystalline p-Si substrate. This result gives evidence for the validity of the PbTe films grown on p-Si substrate by liquid phase epitaxy for several electronic device applications.

The surface morphology of the epilayer of n-PbTe grown on p-Si single crystalline substrates was examined by scanning electron microscopy,SEM . It is clear from the SEM micrograph that a nearly homogeneous dispersion of microcrystals incorporated of PbTe. Prominent features in Fig. 3 are greatly enriched, not identified shapes and rough surface of the grown n-PbTe on p-Si substrate.

3.2 Current density-voltage characteristics

Fig.4 shows the *J–V* characteristics of the n-PbTe/p-Si heterojunction measured in the temperature range 300-400

K. The *J–V* curves are asymmetrical and non-linear. The forward currents follow approximately an exponential trend. The reverse currents observed with negative polarity on the p-Si side are related to the blocking nature of the contact between the n-PbTe films and p- Si substrate. It can be seen that the n-PbTe/p-Si heterojunction shows good rectification effect. This proves that the rectifying effect may be due to the formation of rectifying barrier formed at the n-Pb/p-Si interface. Rectification ratio, RR defined as the ratio of magnitude of forward current to reverse current at certain applied voltage and was found to be 100 at ±1.5 V at 300 K. The rectification ratio increased gradually with increasing the temperature, indicating that electric conduction is dominated by thermal excitation of carriers at voltage-dependent barriers as shown in [18-19].

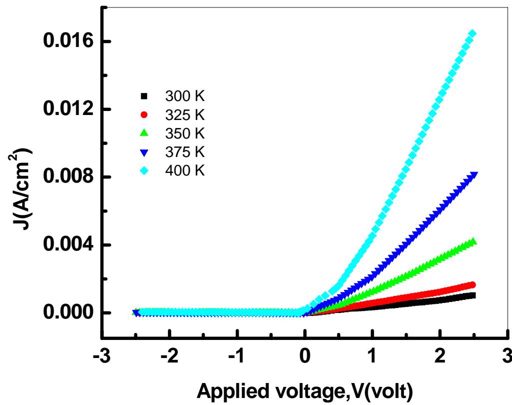

Fig. 4 J-V characteristics of n-PbTe/p-Si heterojunction at different temperatures.

The forward current density (*J*)-forward voltage (*V*) relationship could thus be described by the standard diode equation [17]:

$$J = J_0\left\{\exp\left[\frac{qV}{nkT}\right] - 1\right\}, \tag{1}$$

Where

$$J_0 = A^{*}T^{2}\exp\left(-\frac{q\varphi_b}{kT}\right), \tag{2}$$

and

$$A^{*} = \frac{4\pi q m^{*} k^{2}}{h^{3}}$$

J_0 is the saturation current density, q is the electron charge , V is the voltage, n is the ideality factor, k is the Boltzman constant , T is the absolute temperature, m^* is the effective electron mass , *h is* the Planck constant, and A^* is the Richardson's constant which has a value of A^* is 32 A/(cm^2·K^2) for p-Si [20] .

A semi-logarithmic relationship between the current density and the forward applied voltage was established (Fig. 5). When the applied voltage was changed gradually in the positive direction, the current density followed the exponential trend, but it deviated from the exponential trend at large positive potentials. This is due to a voltage drop across a series resistance (R_S) associated with the neutral region of the semiconductors [21]. So the n-PbTe/p-Si heterojunction appeared to be a non-ideal contact. This is probably due to (a) current crowding, (b) high probability of recombination of electrons and holes in the depletion region, and (c) occurrence of tunneling [22]. It is well known that the downward concave curvature of the forward bias current–voltage plots at sufficiently large voltages is caused by the presence of the effect of R_s, apart from the interface states, which are in equilibrium with the semiconductor [23]. If the series resistance effect is low, the non-linear region will be narrow [24].

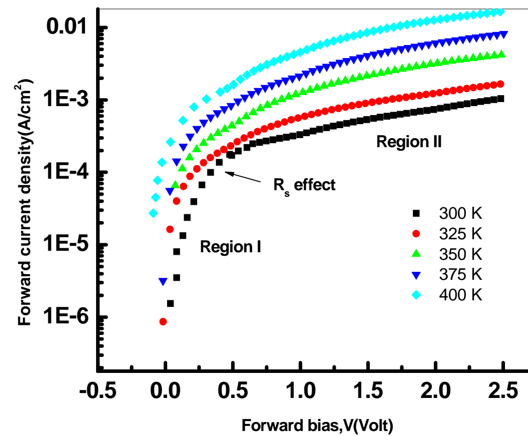

Fig.5 Forward J-V characteristics of n-PbTe/p-Si heterojunction at different temperatures

At large forward voltages, the horizontal displacement ΔV gave a voltage drop IR_S across the neutral region. This resistance limits the exponential behavior of the n-PbTe/p-Si to voltages less than 1.2 V. The current density is related to the applied voltage at high voltages (V > 0.5 V) by the equation [24]:

$$J = J_0\,\{\exp[(q(V - IR_s)/nKT] - 1\} \tag{3}$$

However, Fig.5 could be used to determine R_s of the junction [24]. Thus, for a given *J*, the horizontal displacement between the actual curve and the extrapolated linear part gives the voltage drop, ΔV=(R_s, across the neutral region. The plot of ΔV vs. I shown in Fig. 6 should give a straight line whose slope yields the value of R_s . The temperature dependence of R_s in the as

shown in Fig. 7. This figure is clearly indicate that the high temperature dependence of series resistance in the studied junctions. This means that the series resistance has the main contribution in the junction temperature of our devices.

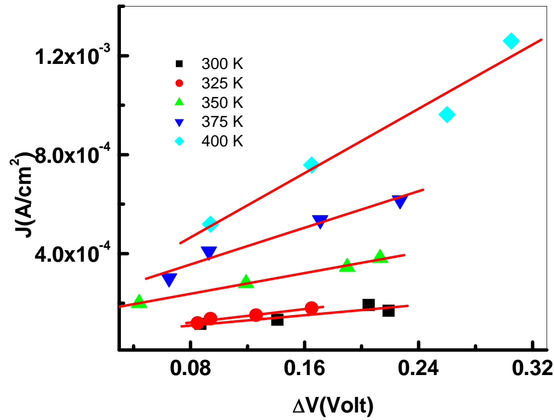

Fig.6 Forward J-ΔV characteristics of n-PbTe/p-Si heterojunction at different temperatures

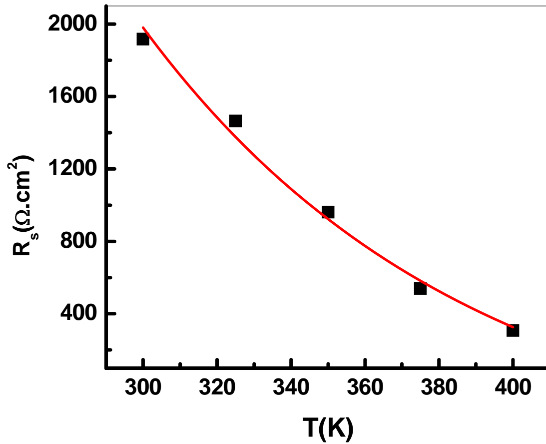

Fig.7 Temperature dependence of R_s for n-PbTe/p-Si heterojunction .

In the first region, for applied voltages lower than 0.2 V , the parameters J_0 and n can be readily determined by a reasonably good fit of the data of the first region of Fig. 5. It is clear from this figure that the junctions within this voltage range have n > 1 , which may be attributed to the recombination of electrons and holes in the depletion region, and also to the increased effect of the diffusion current on increasing the applied voltage [25].

The temperature dependence of the reverse saturation current and the ideality factor is shown in Fig. 8. The significant increase of the saturation current density and decrease of ideality factor with increasing temperature are possibly caused by barrier height inhomogeneities resulting from variation in thickness and non-uniformity of the interface [24-26]

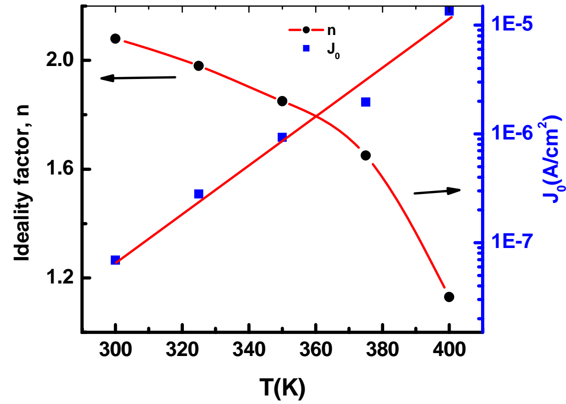

Fig. 8 Temperature dependencies of n and J_0 at low voltage region

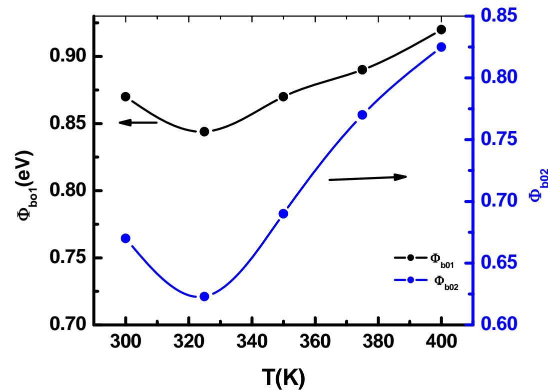

Fig. 9 Temperature dependencies of Φ_{b01} and Φ_{b02}

The temperature dependencies of the barrier heights obtained from the linear fits of the current density –voltage characteristics in the two regions are obtained in Fig.9

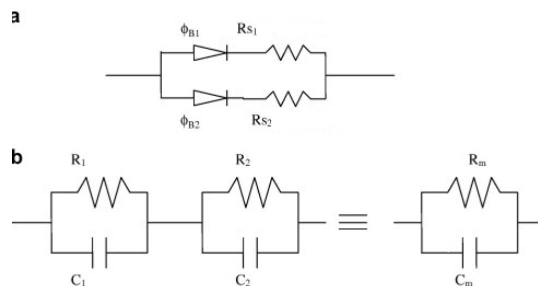

Fig.10 (a) Electric model for two barrier heights (b) The equivalent dynamic circuit of studied Schottky diode.

As the temperature increases, the dominant barrier heights in the two cases will increase with the temperature. This may be attributed to the the spatially inhomogeneous barrier heights and potential fluctuations at the interface that consists of low and high barrier areas [27,28].This behavior can be schematized with the electrical equivalent circuit reported in Fig. 10(a) consisting of two parallel Schottky barrier with the influence of the series resistance for each diode. In the proposed model, the total thermionic current consists of two independent contributions: the first one is related to a rectifier with a high Schottky barrier height and the second one to a rectifier with a low Schottky barrier height, both connected in parallel with the influence of the series resistance for each diode. Thus behavior can be due to different phenomena. Structural defects were investigated such as micro pipes, etch pits, comets on the studied Schottky diodes and presented elsewhere [29]. Further investigations will be performed to find out whether these defects are responsible for the electrical anomalies. A clear correlation between these defects and barrier inhomogeneities cannot be asserted and the effect of Schottky contact will probably be responsible for this effect. In fact, the strength and nature of chemical bonding play a key role in formation interface electronic properties as mentioned by Brillson et al. [30]. A numerical simulations of junction termination extension (JTE) in some Schottky diodes [31] concerning the design of single- and double-zone and its effect on breakdown voltage can also explain the anomalous electrical behavior.

3.3 Capacitance –voltage characteristics

Fig. 11 shows the frequency dependence of the measured capacitance in the frequency range 10^2–10^4 Hz without bias voltage. As observed, the capacitance tends to a constant value at high frequency. This behavior is represented by the simple equivalent circuit shown in Fig. 10(b) of the Schottky diode. R_1 is the bulk series resistance and C_1 its associated capacitance, R_2 and C_2 are the resistance and capacitance, respectively of the Schottky barrier [29,32]. R_m and C_m the equivalent measured parallel resistance and capacity.
A simple equivalent circuit analysis shows that:

$$R_2 = \frac{X^2 + \omega^2 Y^2}{X} \tag{4}$$

And

$$C_2 = \frac{Y}{X^2 + \omega^2 Y^2} \tag{5}$$

Where

$$X = \frac{R_m}{1+\omega^2 R_m^2 C_m^2} - \frac{R_1}{1+\omega^2 R_1^2 C_1^2} \tag{6}$$

And

$$Y = \frac{C_m R_m^2}{1+\omega^2 R_m^2 C_m^2} - \frac{C_1 R_1^2}{1+\omega^2 R_1^2 C_1^2} \tag{7}$$

R_1 was obtained at the frequency of measurements by measuring the current in phase with the applied ac voltage when the diode is biased far in to forward bias. For C_1, we have taken the geometrical capacitance as measured at high frequency.

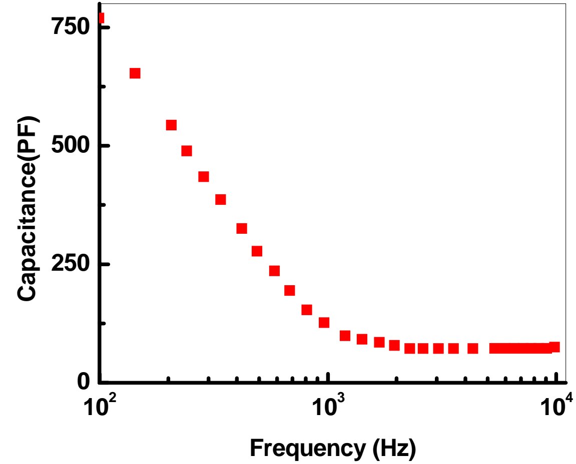

Fig.11 Frequency dependence of capacitance

For some devices having two Schottky barriers at room temperature, we observe a higher value of R_2 and C_2 compared to the one having only one barrier showing the effect of defects probably in Schottky contact. In fact, deep levels localized near these surfaces and interfaces that can dominate the charge transport and transfer properties of n-PbTe/p-Si device. Thus may be explaining that variations in the ratio of low barrier area to the high barrier area lead to the lack of uniformity in the behavior of various samples.

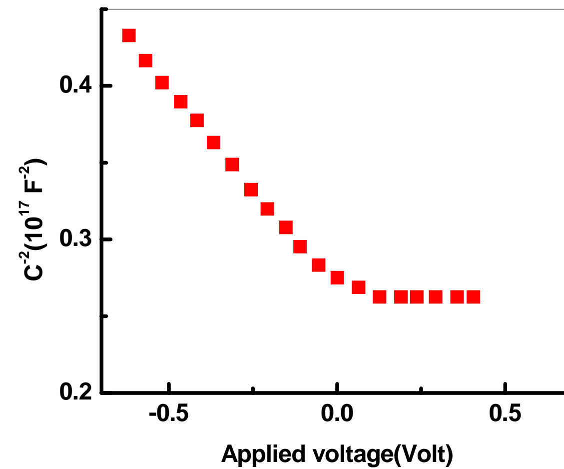

Fig. 12. Plot of $1/C^2$ vs. applied voltage, V

Fig. 12 shows the C^{-2}–V characteristics of the n-PbTe/p-Si device measured in dark at room temperature

(300 K) and at increment voltage of frequency 1 MHz. Accordingly, the total capacitance of the device can be expressed by two capacitors, which give supports the above discussion, one corresponds to the junction capacitance and the other to the geometrical capacitance.

4. Conclusions

The study of the structural and morphology by means of XRD and SEM for the fabricated PbTe films on single crystalline p-Si substrates by LPE gives evidence for the quality of the growth process. *J–V* measurements in the temperature range 300-400 K clarified that the heterojunction behaves like Schottky diode. An interesting feature has been found for our devices which present a current–voltage characteristic represented by two barrier height model due probably to the defects in the bulk or to the Schottky contacts. The capacity behaviour at low frequency exhibits the possibility

to describe the Schottky diode by dynamic electric model consisting of two RC components. The parameters values of the RC components relative to the Schottky barrier were higher in case of device having two Schottky barrier heights due probably to the effect of barrier inhomogeneities. Indeed chemical bonding due to lattice mismatch may be playing a key role in the interface electronic properties.

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