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Invited Paper

Stress, strain, and heterogeneous integration for III-V and II-VI compound semiconductor structures

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The stresses and strains developed through heterogeneous integration of semiconductor structures represent engineering variables for which the materials limits must be addressed. The objective here is to engineer the stability of III-V and II-VI based wafer bond templates for subsequent epitaxial growth of device structures using non-compliant layers. Stress and strain are key parameters in the development of these structures. The difference in coefficients of thermal expansion between the handle substrate and the transferred and subsequently grown layers lead to high strains that can exceed critical thickness values. An empirical model is proposed to explain the experimental data for a series of different template layer / handle substrate combinations. The strain introduced during hydrogen implantation, which promotes exfoliation of a layer, also shows interesting materials-related trends, and the monitoring of the strain helps predict optimal transfer conditions. In both cases, the trends are consistent for a variety of compound semiconductor materials.

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1. Introduction

The feasibility of employing heterogeneous materials integration to leverage device performance has been practiced for over twenty years. Early efforts focused on transferring III-V device structures to an alternative substrate using various lift-off processes [1-3] and more recently, silicon-on-insulator (SOI) substrates have become widely used for advanced semiconductor processing. Analogues of SOI using III-V or II-VI materials have been far less studied but the use of heterogeneous epitaxial materials systems – in applications such as III-V solar cells on Ge substrates [4-6] and CdZnTe buffer layers on Si substrates [7,8] – as well as the drive for higher mobility transistor structures indicates that there is a necessity for such structures. A typical template structure, therefore, consists of a layer of one material (template layer) transferred to a different (handle) substrate. A schematic of the structure is shown in Figure 1. In some cases, electrical transport across the interface is important, but in many cases, as in the SOI case, the template layer is intentionally isolated from the handle layer. Recent efforts in this area [9-13] have indicated that such structures can be produced and device quality layers [14] can be achieved on such structures.

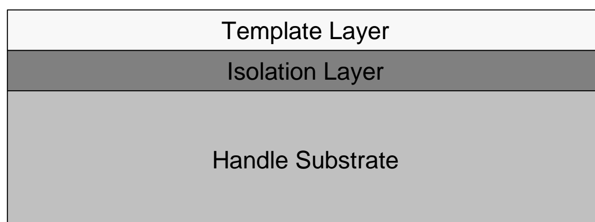

Fig. 1. Schematic diagram of the wafer bonded structures. The isolation layer thickness is approximately 100 nm and the template layer thickness varies from 0.3 to 50 μm.

Constraints on the use of these so-called "template substrates" are based on the materials systems employed. The constraints that will be addressed here include (i) differences in the coefficients of thermal expansion (CTE) between the handle substrate and the transferred layer and (ii) the mechanism by which the template layer can be removed from one substrate and transferred to another. Stress and strain are key issues in both of these processes. Lattice mismatch is an important issue in heteroepitaxial growth, but this issue is not a factor for the template structures described here. However, strain, in the form of CTE differences between the handle substrate and template layer, remains an issue and the equivalence of a "critical thickness" must be determined to best utilize the templates. Transfer of a template layer from one substrate to another is typically achieved by either a bond-and-etch method, similar to the process by which SOI wafers were initially produced [15] or by an "ion cut" technique [16,17] in which the layer is exfoliated from the original substrate by ion implantation of hydrogen (or other species) and subsequent annealing. This process is also a commercially viable process for SOI transfer. However, the evolution of hydrogen and point defects in an implanted structure is strongly materials-dependent and determination of trends by which this process occurs in different III-V and II-VI materials would be very useful. These constraints will be explored for both III-V and II-VI systems.

2. Experiment

The experiments described utilized semi-insulting or non-intentionally doped substrates. For the III-V materials (and silicon), (001) oriented commercial wafers are employed, whereas (211) oriented $Cd_{0.96}Zn_{0.04}Te$ substrates are used [18]. The III-V and Si wafers are

500-600 μm thick and the CdZnTe substrate is 1 mm thick. In all cases described here, SiN is deposited on both wafer surfaces and the surfaces are "activated" using low power oxygen plasma.[11,19] After activation, the wafers are bonded through a single pressure point at room temperature. Two layer transfer techniques were investigated in this study. The first is a bond and etch back approach where after bonding and annealing at low temperature (to strengthen the bond, 150 °C) the bulk of the transfer wafer is removed by grinding, etching and polishing until only approximately 10 microns remain. The thinned samples were then annealed at higher temperatures, for 1 hour time intervals, to assess the effects of their CTE mismatch. The second thinning process used here is the "ion cut" technique. Prior to bonding the transfer wafer is implanted with H_2^+ ions at a dose of 2.5×10^{16} cm^{-2} and energy of 150 keV. Some wafers were intentionally cooled during this sequence (GaAs, InP, InAs at 253K; CdZnTe at 77K, others nominally at room temperature). After bonding, the pair is then annealed at a lower temperature (which is dependant upon the material) and then at a higher temperature (also materials dependent) to achieve exfoliation of the hydrogen implanted wafers and transfer to the handle wafer.

High resolution x-ray diffraction (including triple axis diffraction (TAD) (REF from our group), double crystal x-ray topography (DCXRT), transmission electron microscopy (TEM), and atomic force microscopy (AFM) were employed to characterize the structures.

3. Results and discussion

The role of the difference in the CTE for the template layer and the substrate is described through the following experiments. The identification convention is: template / handle, so InP / Si describes an InP template layer on a silicon substrate. The CTE of the materials addressed here do not change appreciably over the limited annealing temperature range employed, so the room temperature values of 2.6×10^{-6} °C^{-1} (Si), 5.7×10^{-6} °C^{-1} (GaAs) and 4.6×10^{-6} °C^{-1}(InP) are used. InP/Si (ΔCTE = 2×10^{-6} °C^{-1}), InP/GaAs (-1.1×10^{-6} °C^{-1}), InP/InP (0), and GaAs/Si (2.9×10^{-6} °C^{-1}) combinations are presented here to include a range of values, both positive and negative.

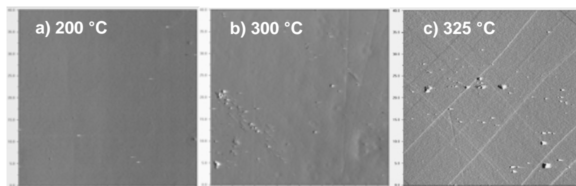

Fig. 2. AFM images from InP template layers on silicon substrates after annealing at a) 200 °C, b) 300 °C, and c) 325 °C.

Fig. 2 shows AFM images from the InP template layer on silicon substrates at different temperatures. In this case, the InP transferred layer is 10 μm thick. At temperatures up to 300 °C, there are no signs of deformation by AFM. However, at 325 °C, a cross-hatch pattern produced by misfit dislocations is observed. Fig. 3 shows InP on GaAs annealed at 325 °C for increasingly thick InP layers. Deformation is not observed for the 10 μm thick layer, but is observed for the layers 50 μm and thicker. Figure 4 compares 10 μm GaAs/Si at 200 °C and 325°C. Here, deformation is observed at 325 °C with a higher defect density than observed in the InP / Si structure annealed at the same temperature. Misfit dislocations are first observed in the 10 μm GaAs / Si structure at temperatures of 250 °C. Although the AFM indicates that there are no defects forming at lower temperatures, DCXRT, which is very strain sensitive, provides more information. Figure 5 depicts diffraction images from InP/InP, InP/Si, ad GaAs/InP structures annealed at 150 °C and 200 °C for 1 hour each. With greater ΔCTE and higher temperature, the diffraction images show an increasingly equiaxed structure in which it appears that the initial components of deformation are being introduced. For the case where ΔCTE = 0 (InP / InP) no such contrast exists at any temperature.

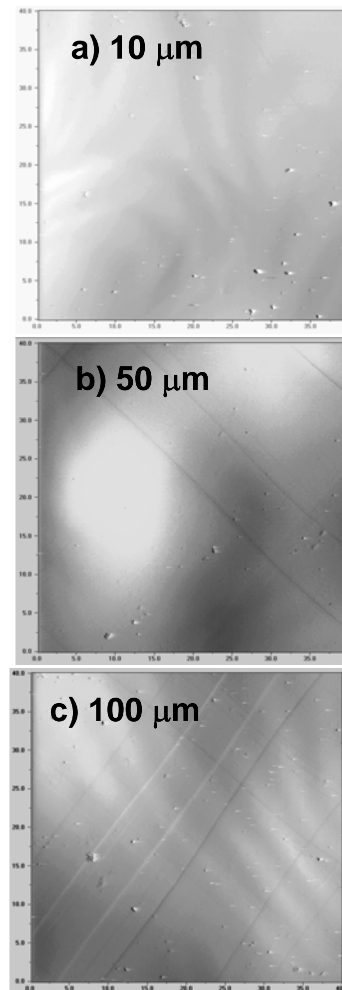

Fig. 3. AFM images from InP template / GaAs handle structures for different thickness InP template layers.

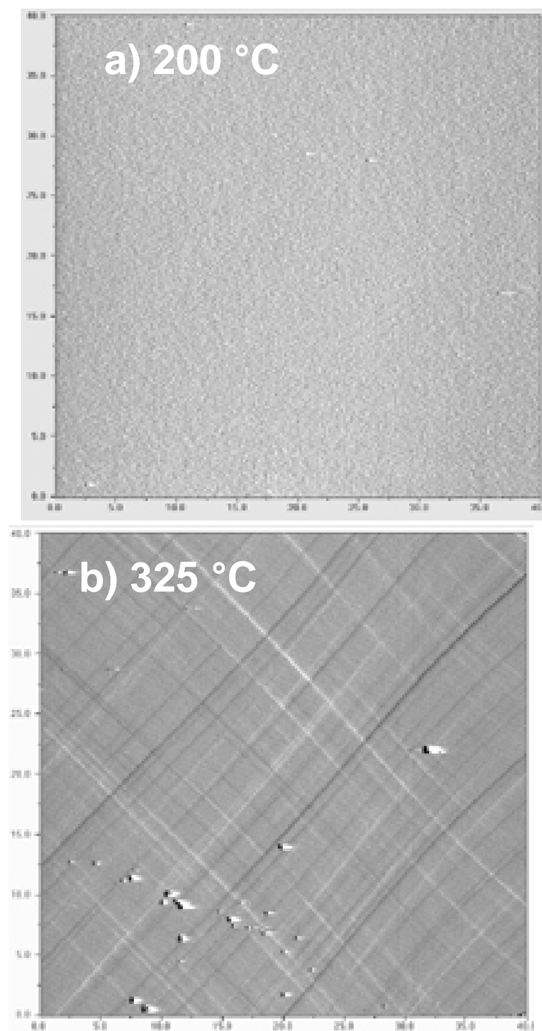

Fig. 4. AFM images from GaAs template / Si substrate structures after annealing at a) 200 °C and b) 325°C.

The information from these structures as well as from thinner layers on substrates demonstrates that one can approximate the stability of the bonded pairs with information about the template layer thickness, ΔCTE, and temperature. Although there is an effort to provide a more precise model to predict the stability regime for heterogeneous bonded structures over a wide temperature range, a useful empirical formula is expressed in terms of strain and layer thickness (provided the layer is somewhat thinner than the handle substrate) in a modified Matthews-Blakeslee formulation. For low temperatures (< 400 °C), where the critical thickness value (which is a thermodynamically defined term) is increased by about a factor of 20 before deformation is observed by AFM. This hindered deformation is due, presumably, to the slow deformation kinetics at lower temperatures. The approximation does hold at higher temperatures, however, as an InAlAs / InGaAs quantum well structure (total thickness < 1.0 μm) epitaxially deposited by metalorganic vapor phase epitaxy at 600 °C on an InP / GaAs structure showed no signs of plastic deformation [14]. The rough model here predicts that the structure would be stable up to a thickness of over 7 μm, although the kinetic processes would be significantly faster at the higher temperatures. Nonetheless, the ability to achieve good quality epitaxial growth on the template structures with a thermal expansion misfit indicates that tolerable levels of thermal-induced strain can coexist with high performance device structures.

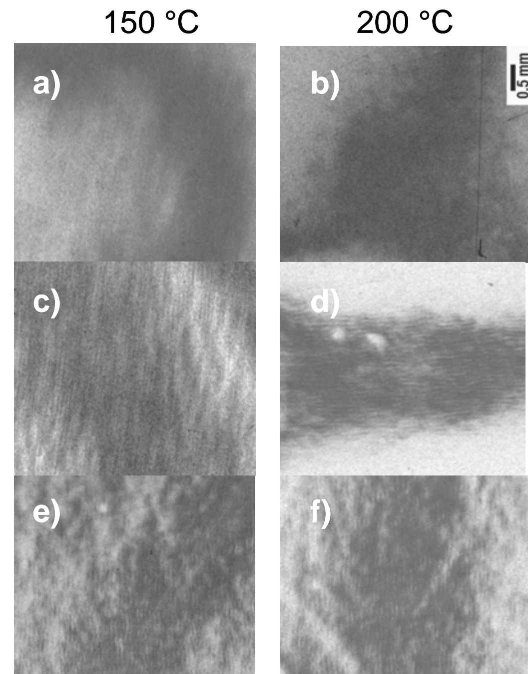

Fig. 5. Double crystal x-ray diffraction images from 10 μm template layers on handle substrates after annealing at different temperatures. a), b): InP / InP; c), d):InP / GaAs; e),f): GaAs / Si.

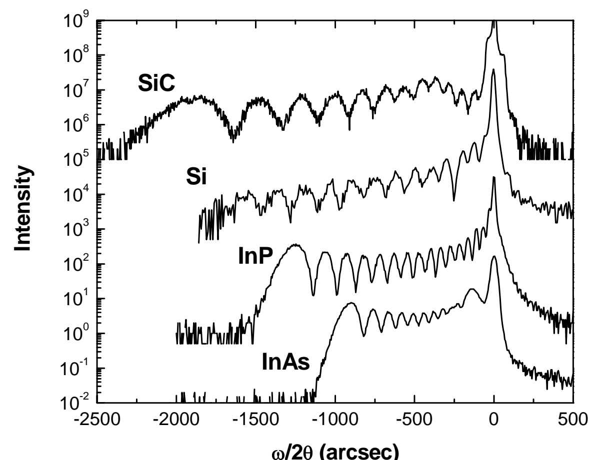

Fig. 6. ω/2Θ diffraction scans for sample implanted with the same hydrogen dose (H2 + 2.5×1016 cm^{-2}) and energy (150 keV).

The means of transferring a layer by bond-and-etch is feasible, but the original wafer is destroyed in the process. The development of hydrogen implantation and exfoliation for silicon has led to the production of SOI wafers. Using the same technique for III-V materials requires knowledge about the kinetics of hydrogen diffusion, agglomeration, and point defect interactions in the semiconductor materials to be used in the process. Efforts have focused on InP,[9,20,21] InAs and $In_xAl_{1-x}As$ graded buffer layers,[10,13] and $Cd_{0.96}Zn_{0.04}Te$.[12] The state of the as-implanted hydrogen has been shown to be an important determinant for the effectiveness of exfoliation and we have developed high resolution x-ray diffraction to characterize the as-implanted structures. The implantation of a high dose of hydrogen into a semiconductor produces a high concentration of interstitial point defects and implanted species in the host lattice. These species act to expand the lattice perpendicular to the surface while the in-plane lattice remains constrained by the bulk semiconductor. During subsequent annealing, diffusion and agglomeration of the hydrogen and point defects leads to the formation of hydrogen platelets. Earlier results have confirmed that high resolution x-ray diffraction is an ideal technique for studying the kinetics of this process with particular emphasis on Si, [22] InP [9,20] and, more recently InAs and GaSb [23].

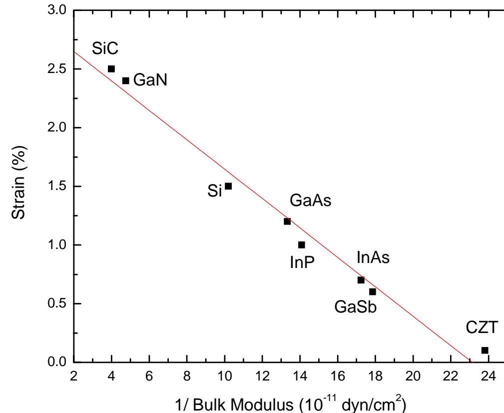

Fig. 7. Plot of strain as a function of inverse bulk modulus for different semiconductors under the same implanted conditions.

A compilation of the strain induced by the implanted hydrogen in a variety of semiconductors shows interesting trends and provides some initial insight into the state of the implanted structures. Figure 6 shows examples of rocking curves from as-implanted layers where successful blistering/exfoliation occurred upon subsequent annealing. For these samples, the implant dose and energy was constant with values of 5×10^{16} cm^{-2} H_2^+ and 150 keV. A series of fringes to the left of the substrate peak is observed in these cases and it has been shown [22] that the diffraction pattern can be used to determine the strain profile in the semiconductor. The strain is positive in all cases, indicating interstitial-type defects are introduced.[24] Our earlier results [20] showed that the strain introduced is proportional to the implant dose. This is consistent with an implantation process in which the damage cascades from the implanted species are isolated. At higher damage levels, intercascade interactions become more prevalent and should lead to a sublinear increase in strain with increasing dose. This finding is interesting given that such high doses of hydrogen are introduced, but the small hydrogen mass clearly limits the damage introduced into the host crystal. Given this process, Figure 7 shows that the strain introduced by the implantation is related to the Bulk modulus for the implanted target.[25] Implanted substrate targets with higher Bulk modulus induce a higher strain. The relationship is roughly linear, as shown in Figure 7, when the induced strain is plotted against the inverse modulus. The universal nature of this process is confirmed as III-V, IV, and II-VI materials fall on the same line.

4. Conclusion

Stress and strain play important roles in understanding stability issues for heterogeneous integration using III-V and II-VI materials. The critical thickness, driven by differences in CTE, follows a similar dependence on strain and layer thickness developed for epitaxial layers, whose strain originates from both lattice mismatch and CTE differences. Strain in hydrogen implanted semiconductors provides a very useful measure of the state of strain of the as-implanted structure. The strain in the implanted layers is introduced by interstitial point defects and the implanted hydrogen species. The level of strain is related to the modulus of the implanted material with higher strain produced in materials with higher modulus values.

Acknowledgements

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