The origin of anomalous peak and negative capacitance in the forward bias C-V characteristics of Au/n-GaAs contacts at low temperatures (T≤300 K)

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Au/n-GaAs contacts were fabricated using n-GaAs wafer with high doping concentration and their electrical characteristics were investigated via admittance measurements at low temperatures (T≤300 K) at 1MHz. The main electronic parameters such as barrier height, depletion region width, doping concentration, series resistance and Fermi energy were obtained from experimental data. All these parameters showed dependence on temperature since different conduction mechanisms may play role at a certain voltage and temperature range. The forward bias capacitance-voltage curve exhibited an anomalous peak and then capacitance took negative values for each temperature. Such negative capacitance behaviour can be explained by the loss of interface charges located at junction, the existence of surface states, series resistance and a native interlayer. The decrease in series resistance and increase in surface states with increasing temperature were attributed to the decrease in band gap of GaAs and restructuring and reordering of surface charges.

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1. Introduction

Gallium arsenide (GaAs) devices have high saturation velocity, high electron mobility, large/direct bandgap, and break-down voltage [1]. These structural properties give them the opportunity of being used as a basic component for high speed electronic, optoelectronic and high-speed microelectronic applications in the experimental studies of semiconductor devices [1,2]. The fabrication process of the metal-semiconductor (MS) with and without an interfacial layer, sample temperature, electric field, frequency, series resistance (R_s), surface states (N_{ss}), and band gap energy (E_g) are very important because they affect conduction mechanisms in the device and play an important role regarding the performance and reliability of the device [3-8].

In general, above room temperatures (T≥300 K), the main dominant conduction mechanism is thermionic emission (TE), but many different conduction mechanisms may make contribution to current in a way that one or more mechanisms become dominant for a certain voltage and temperature range particularly below room temperature. Therefore, the investigation of electrical characteristics in these structures at low temperatures is quite complicated. In this respect, many experimental studies on metal-GaAs (MS) contacts have been conducted for enhancing the device quality [9-15]. On the other hand, theoretical analysis of the conduction mechanisms is difficult especially at low temperatures for reliable information on the formation of barrier height (BH) at M/S interface and possible conduction mechanisms [16-19].

However, the capacitance and conductance data under reverse bias can be used to obtain information about the Schottky device parameters such as BH, conduction mechanism, the depth of depletion layer and etc. It is supposed that the depletion region of an ideal Schottky structure behaves in some respects like a parallel-plate capacitor [4]. However, there are many factors that can cause the device deviate from the ideal structure in practice. These factors are classified under two main groups: material and fabrication process. The semiconductor type and impurity concentration of the semiconductor and other related material properties are in first group. The cleaning process of semiconductor surface and the calibration of evaporation process to form rectifying contact that affects BH inhomogeneity at the M/S interface, density distribution of N_{ss} or dislocation and R_s can be considered in the second group [2-4]. These also serve as the factor that is responsible for the charges at interface states/traps and surface polarization, which are important for the variation of main diode parameters with varying frequency, voltage and temperature [1-10]. Here, temperature needs particular attention because the analysis of the reverse bias characteristics of a contact only at room temperature by using capacitance-voltage (C-V) and conductance-voltage (G/ω-V) measurements cannot provide detailed information on the barrier formation, conduction mechanisms, and capacitor behaviour at M/S interface.

There are various studies in the literature on negative capacitance (NC) phenomena for several device types [20]. These studies basically reports a decrease in capacitance which finally becomes negative in the accumulation region. This indeed means that the device performs inductive behaviour; thus charge density on the metal contacts is lowered by increasing bias voltage. Jonscher [21] utilized the time-domain explanation and associated NC with a rising current-time dependence. Wu et al. [22] explained NC through waterfall analogy by pointing out a charge delocalization mechanism due to the impact of hot carriers with trapped charge carriers. Werner [23] provided an opposing view and stated that NC stems from defective back contacts. On the other hand, Zhu et al. [24] revealed radioactive recombination in the active region can lead to NC phenomena in LEDs. As the origin of NC for different types of devices varies, this phenomena have been given great attention in the last decade [25-29].

This study focuses on the investigation of anomalous peak and negative capacitance in C-V characteristics of the Au/n-GaAs contacts using the experimental C-V-T and G/ω-V-T data. For this purpose, admittance measurements of the contacts were performed in wide range of applied bias voltage at 1 MHz. All measurements were repeated between 80 K and 300 K in order to characterize device below room temperature. The observed NC behaviour and anomalous peak in the forward bias/accumulation region was explained by the loss of interface charges located at junction, the existence of N_{ss} and their relaxation time, R_s and a native interlayer.

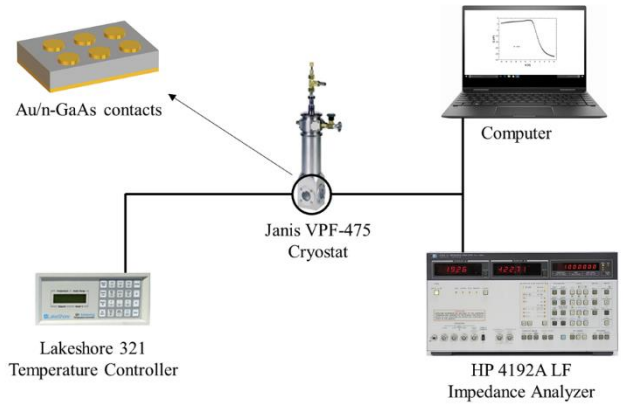

Fig. 1. Schematic diagram of Au/n-GaAs contacts and the measurement system (color online)

2. Experimental details

Au/n-GaAs junctions were fabricated using n-GaAs wafer with diameter of 5.08 cm, orientation of (100), thickness of 350 μm, and doping concentration ~2×10^{18} cm^{-3}. Before the fabrication process, n-GaAs wafer was dipped in ammonium peroxide for 40 seconds to remove native oxide layer on the surface and then was etched in sequence with acid solutions (H_2SO_4:H_2O_2:H_2O=3:1:1) for 60 s, and (HCl:H_2O=1:1) for another 60 s in the ultrasonic bath. Later, the wafer was again rinsed in deionized water with 18 MΩ resistivity and was dried immediately by nitrogen gas. After cleaning the wafer, high purity Au (99.995%) with thickness of ~1500 Å was thermally evaporated from the tungsten filament on the whole back side of it at about 10^{-6} Torr in high-vacuum system. In order to achieve good an ohmic contact, Au coated wafer was sintered at 500 °C for 5 min in a nitrogen atmosphere. After, Au rectifying contacts with diameter of 1 mm and thickness of 1500 Å were deposited on the front side of n-GaAs wafer through a metal shadow mask in the metal evaporation system. For electrical measurements, Au/n-GaAs contacts were was mounted on a copper holder with the help of silver paste and the electrical contacts were made to the upper electrodes using thin silver coated wires with silver paste.

The schematic diagram of Au/n-GaAs contacts and measurement system was given in Fig.1. C–V and G/ω–V measurements were performed in the temperature range of 80-300 K at 1 MHz by using an HP 4192A LF impedance analyzer and test signal of 40 mV_{rms}. All these measurements were carried out in the temperature controlled Janis vpf-475 cryostat and the temperature was monitored by Lakeshore model 321 auto-tuning temperature controller with the help of a microcomputer through an IEEE-488 AC/DC converter card.

3. Results and discussions

C-V and G/ω-V characteristics of Au/n-GaAs contact are given in Fig. 2 (a) and (b), respectively. It is clear that the C-V and G/ω-V characteristics of Au/n-GaAs contact strongly depend on applied bias voltage. Moreover, the dispersion for different temperature levels indicates dependence on temperature to some level. Such dependence of the capacitance and conductance can be attributed to the spatial density distribution of trapped charges and their relaxation time (τ), series resistance, a native interfacial insulator layer, and hopping mechanisms between these traps or conduction band under temperature and electric field effects [1-6,17-19,30,31].

Another important result that is observed is the existence of NC capacitance and anomalous peak in the accumulation region and the minimum value of C in this region corresponding with the maximum of the G/ω for each temperature. Au/n-GaAs contacts's NC behaviour would not be an unexpected behaviour considering NC is often encountered at low temperatures and high frequencies [22] yet some other structures exhibited NC either for high and low frequency regions both [29] or for only low frequency region [25]. In the case of Wu and his colleagues' explanation, electrons at the interface with higher energy impact with trapped electrons and this vacates the trap which is later filled by an electron from the metal contact [22]. Similarly, Perera et al. [31] fabricated a detector with layers of GaAs and associated the NC behaviour with the carrier capture and emission from the interface states. Thus, NC behaviour could be utilized for reducing capacitance of the circuit so that decreased response time could be obtained through circuit's lower RC constant owing to NC [31].

Besides, NC can be useful for negating capacitances in an antenna, boosting voltages at various part of a circuit, and developing coil-free resonators and oscillators [27] whereas it causes reduction of the photoconversion efficiency solar cells [28].

In another study, Vural et al. [26] fabricated Al/n-GaAs structure with rhodamine-101 interlayer and attributed NC phenomena to the injection of charge carriers which involves a process of hopping to localized interface traps/states. In most cases, if particular attention was not given, very thin native interfacial layer could be formed at M/S interface of the Au/n-GaAs and such layer would yield states/traps which store and release charge carriers. This could also play a part in appearance of NC behaviour. Since capacitance is associated with dielectric constant, NC also affects dielectric constant which would take very low values in a particular bias voltage range and negative beyond it [29]. It needs to be noted that dielectric constant would become positive at low frequencies for some structures or at high frequencies. In such case, these structures behave as charge or energy storage devices for a specific frequency range whereas they act as an energy source in the circuit for the frequency range where NC is observed. As to the observed peak behaviour of the C and G/ω in Fig. 2(a) and 2(b), this can be attributed to the increments in the polarization and more carriers in the MS contact, the existence of R_s, N_{ss} and the formation of a native insulator layer at Au/n-GaAs interface.

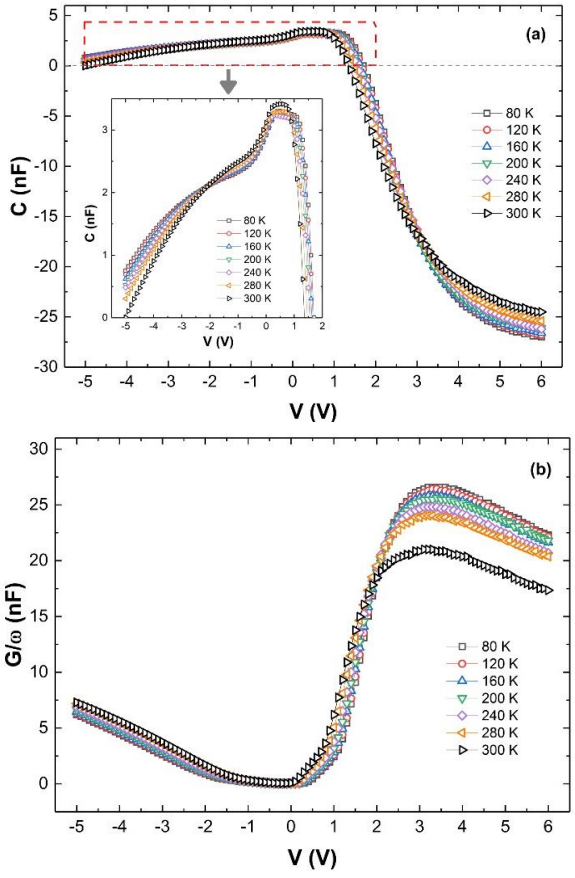

Fig. 2. (a) C-V graph (b) G/ω-V graph of Au/n-GaAs contacts (color online)

In addition, the change in capacitance with voltage appears to be similar for different temperature levels. It is clearly seen in the inset of Fig. 2(a) that the capacitance increases with an increment in bias because of accumulation of same type carriers between -5 V and 0 V [4]. After 0 V the surface becomes devoid of any carriers leaving only the depletion layer. This goes on until ~2 V and then there is a tendency at the surface to invert the conductivity type. This corresponds to depletion and inversion regions [30,31]. The change in G/ω according with bias voltage is also seen clearly in Fig. 2 (b) such that the changes in capacitance and conductivity are in consistency with each other. The conductivity decreases at a certain voltage range in which the capacitance is increased with bias voltage or vice versa [30,32]. The voltage and temperature dependence of capacitance and conductance is attributed to series resistance and particular distribution of interface states between semiconductor and oxide layer [31-33]. R_s can originate from the back ohmic contact to the semiconductor, the contact made by the probe wire to the gate or rectifier contact, the bulk resistance of the semiconductor, particulate matter at back contact interface and quite non-uniform doping concentration of donor or acceptor atoms in the semiconductor [33,34].

The existence of R_s in MIS/MOS and MPS type structures leads to serious error in the calculation of main electrical parameters of these structures, but it can be minimized by sample fabrication, measuring R_s and applying a correction the measured C/G-V plots especially for high frequencies (f≥500 kHz) before desired information is extracted. Theoretically, when these structures are biased into strong accumulation, the admittance is given by $Y_{ma} = G_{ma} + j\omega C_{ma}$ [30]. Using the real and imaginary parts of the admittance, the value of series resistance for these structures can be calculated by using following relation [30].

$$R_s = \frac{G_{ma}}{G_{ma}^2 + \omega^2 C_{ma}^2} \quad (1)$$

Thus, the values of R_s was also calculated using Eq. (1) as a function of bias voltage at various temperatures and given in Fig. 3.

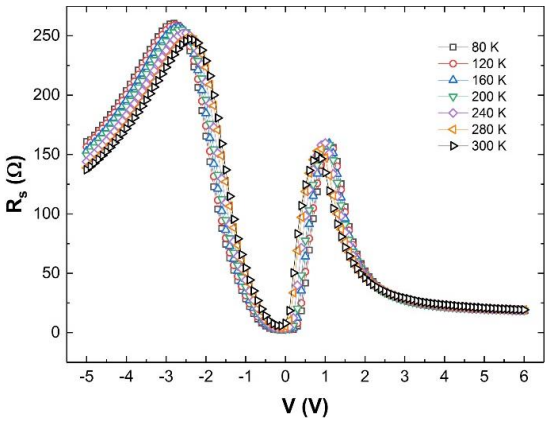

Fig. 3. R_s-V graph of Au/n-GaAs contacts (color online)

In Fig. 3, there exists two peaks in R_s-V-T profile: at about -2.2 V and 1.1 V. In terms of peak points, there exists meaningful relationship between C-V-T and R_s-V-T profiles because there is an intersection point in C-V-T profile at -2.2 V. In other words, capacitance decreases until -2.2 V as the temperature is increased, but capacitance decreases again after -2.2 V as the temperature is increased. Similar effect is available for the other peak point (at 1.1 V) as well. Thus, accumulation, depletion and inversion regions in C-V-T and G/ω-V-T are in good agreement with each other and with series resistance characteristics. The decrease in G values is also suitable with the slight increase in R_s. However temperature dependence of these parameters is not as strong as their dependence on bias voltage as seen in Fig. 4. Such behaviour of C-V-T and R_s-V-T profiles can be attributed to an inhomogeneous interfacial layer because of the interface states at the GaAs surface.

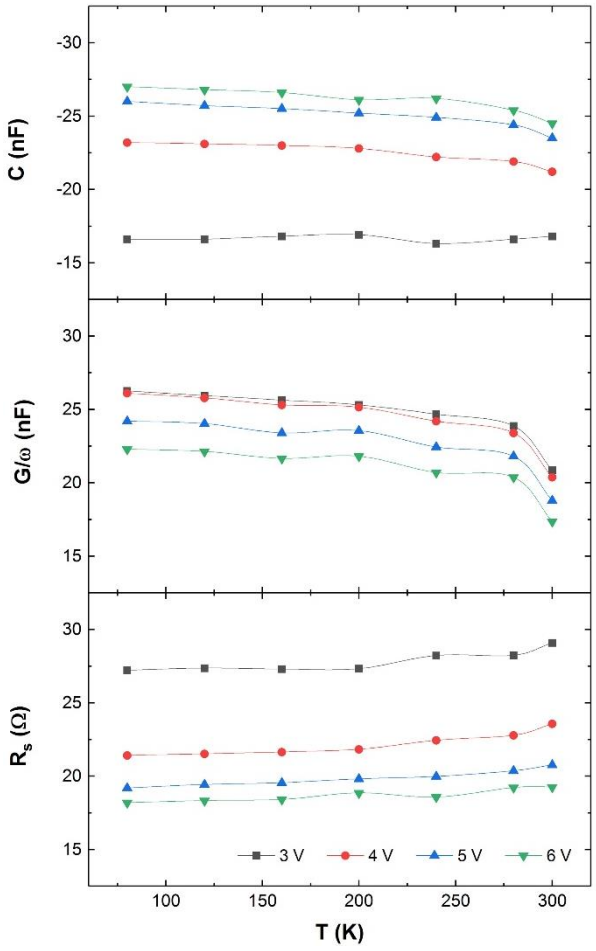

Fig. 4. C-T, G/ω-T and R_s-T graphs of Au/n-GaAs contacts (color online)

Some of the device parameters were also obtained using C^{-2}-V data in the following relation [3,4];

$$C^{-2} = \frac{2(V_R + V_o)}{q\varepsilon_s\varepsilon_o N_D A^2} \quad (2)$$

where A is the diode's cross-sectional area, V_R is the applied reverse bias, V_o is the voltage value that corresponds to intercept of C^{-2}-V plot, N_D is the donor concentration, ε_s is the dielectric constant of GaAs, and ε_o is the permittivity of free space (=8.85x10^{-14} F.cm^{-1}).

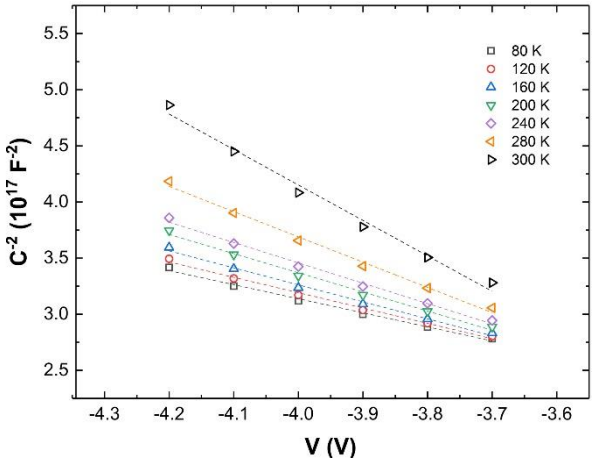

Fig. 5. C^{-2}-V graph of Au/n-GaAs contacts (color online)

As can be seen in Fig. 5, C^{-2}-V characteristics for each temperature can be fitted with straight lines. Thus, an intercept voltage, V_o, for each temperature was determined from C^{-2}-V characteristics. Moreover, the slope of linear fit was also extracted so that the values of N_D were calculated for each temperature by using Eq. 2. The values of diffusion potential, V_D, were also calculated using following equation.

$$V_D = V_o + \frac{kT}{q} \quad (3)$$

Here, k is the Boltzmann constant and T is temperature in Kelvin. Fermi Energy Level (E_F) were obtained using following equation [1,2];

$$E_F = \frac{kT}{q} Ln\left(\frac{N_C}{N_D}\right) \quad (4)$$

where, N_C is the effective density of states in GaAs conduction band and the values of N_C can be calculated using following equation [1,2];

$$N_C = 2\left(\frac{2\pi m_e^* m_o k}{h^2}\right)^{3/2} T^{3/2} \quad (5)$$

Here m_e^* is the effective mass of electron (0.067 of GaAs), m_o is the rest mass of the electron, h is the Planck's constant [9-12]. Thus, some device parameters such as V_D, N_D, N_C and E_F were calculated and given in Table 1.

Table 1. Experimental values of V_D, N_D, N_C and E_F for Au/n-GaAs contacts

T	V_D	N_D	N_C	E_F
(K)	(V)	(cm^{-3})	(cm^{-3})	(meV)
80	1.771	$4.56x10^{16}$	$6.01 x10^{16}$	1.92
120	1.905	$3.80x10^{16}$	$1.10 x10^{17}$	11.10
160	2.096	$3.09x10^{16}$	$10.7 x10^{17}$	23.5
200	2.253	$2.56x10^{16}$	$2.38 x10^{17}$	38.4
240	2.375	$2.33x10^{16}$	$3.13 x10^{17}$	53.7
280	2.588	$1.66x10^{16}$	$3.94 x10^{17}$	76.5
300	2.633	$1.02x10^{16}$	$43.7 x10^{17}$	97.2

Schottky type structures has depletion layer formed at the junction of a metal and semiconductor. According to Schottky-Mott theory, if metal and n-type semiconductor connected electrically, electrons pass from the semiconductor into the metal and the two Fermi levels are forced to coincidence [4]. There is a negative charge on the surface of the metal balanced by a positive charge in the semiconductor; hence an electrical field from n-type semiconductor to metal is formed [4]. The positive charges in the semiconductor are provided by conduction electrons receding from the surface, leaving uncompensated positive donor ions in a region depleted of electrons. These uncompensated donors occupy a layer of appreciable thickness, W_D [4]. The width of depletion region (W_D) was obtained by using following equation [3];

$$W_D = \left(\frac{2\varepsilon_s \varepsilon_o V_D}{qN_D} \right)^{1/2} \tag{6}$$

Thus the barrier height (Φ_B) for each temperature for Au/n-GaAs contact were obtained using following equation [1,2];

$$\Phi_B = c_2 V_o + \frac{kT}{q} + E_F - \Delta\Phi_B \tag{7}$$

where, $\Delta\Phi_B$ is image force barrier lowering which is given by [1,2];

$$\Delta\Phi_B = \left(\frac{qE_m}{4\pi\varepsilon_s \varepsilon_o} \right)^{1/2} \tag{8}$$

Here, E_m is maximum electrical field which is obtained by using the equation below;

$$E_m = \left(\frac{2qN_D V_d}{\varepsilon_s \varepsilon_o} \right)^{1/2} \tag{9}$$

Because the interface states are in equilibrium with the semiconductor, contribution of interface states to structure capacitance is lowered particularly at high frequencies [3,4]. A practical method for obtaining N_{ss} is to utilize ratio of experimental donor concentration, N_D, to theoretical donor concentration, N_D'. This ratio is referred as c_2 which is given by following equation [3,4];

$$c_2 = \frac{N_D}{N_D'} = \frac{1}{1 + \frac{qd_{ox}N_{ss}}{\varepsilon_i}} \tag{10}$$

Interface state density value for each temperature was calculated by using Eq. 10 where N_D' is equal to $7.35x10^{16}$ cm^{-3}. Here, d_{ox} was calculated following equation [35];

$$C_{ox} = C_{ma}\left[1 + \left(\frac{G_{ma}}{\omega C_{ma}} \right)^2 \right] = \frac{\varepsilon_i \varepsilon_o A}{d_{ox}} \tag{11}$$

The values of Φ_B, E_{max}, W_D, c_2, N_{ss} and R_s for each temperature are given in Table 2. As seen in the table, the values of W_D, N_{ss} and R_s increase with increasing temperature whereas opposite behaviour is observed for Φ_{CV} and c_2. Using the values in Table 2, temperature profiles of Φ_B and N_{ss} were obtained and plotted as Φ_B–T and N_{ss}–T graphs given in Figs. 6 and 7.

Table 2. Main parameters of Au/n-GaAs contacts obtained from C^{-2}-V characteristics

T	Φ_B	E_{max}	W_D	c_2	N_{ss}
(K)	(eV)	($V.cm^{-1}$)	(cm)		($eV^{-1}.cm^{-2}$)
80	1.10	$1.49x10^5$	$2.37x10^{-5}$	0.620	$5.46x10^{11}$
120	1.00	$1.41x10^5$	$2.70x10^{-5}$	0.517	$8.34x10^{11}$
160	0.91	$1.34x10^5$	$3.14x10^{-5}$	0.420	$1.23x10^{12}$
200	0.84	$1.26x10^5$	$3.57x10^{-5}$	0.348	$1.66x10^{12}$
240	0.82	$1.24x10^5$	$3.84x10^{-5}$	0.317	$1.92x10^{12}$
280	0.68	$1.09x10^5$	$4.75x10^{-5}$	0.226	$3.06x10^{12}$
300	0.49	$8.62x10^4$	$6.11x10^{-5}$	0.139	$5.52x10^{12}$

As can be seen Fig. 6, barrier height changes almost linearly with temperature according to the following equation [36,37];

$$\Phi_B = \Phi_B(T=0) + \alpha T \tag{12}$$

where $\Phi_B(T=0)$ is barrier height at zero temperature and α is temperature coefficient of the barrier height which takes negative value. This parameters indicates that the barrier height of the structure is decreased as the temperature is increased which is associated with charge carriers' gaining more thermal energy and their ability surpass the barrier easily. Such negative value for α is also associated with temperature dependence of band gap energy of the semiconductor as well. Linear fit of Φ_B–T revealed the value of α as $2.39x10^{-3}$ $eV.K^{-1}$ whereas that of $\Phi_B(T=0)$ is 1.3 eV. This result is in a very good agreement with the findings of other studies in literature [34-41].

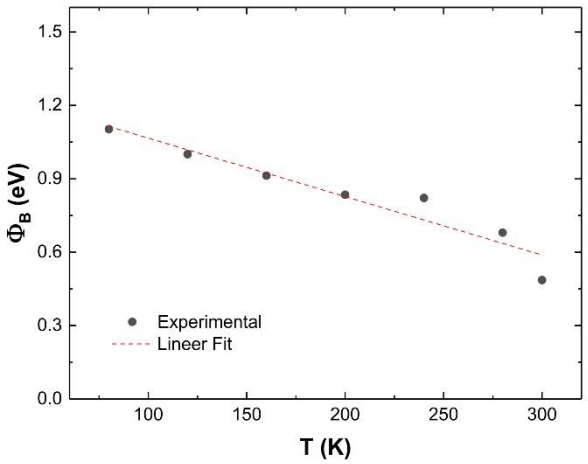

Fig. 6. Φ_B-T graph of Au/n-GaAs contacts (color online)

Fig. 7 shows that the value of N_{ss} increases with increasing temperature. The effect of temperature on interface states is probably due to the increase of the defects at the semiconductor-metal interface. The termination of the bulk periodic potential of a solid at its surface leads to surface states whose wave-functions decay exponentially into the bulk [4]. The energy levels associated with these defects may lie in the band gap of the semiconductor, where they may act like surface states and lead to pinning of the Fermi Level [3,4].

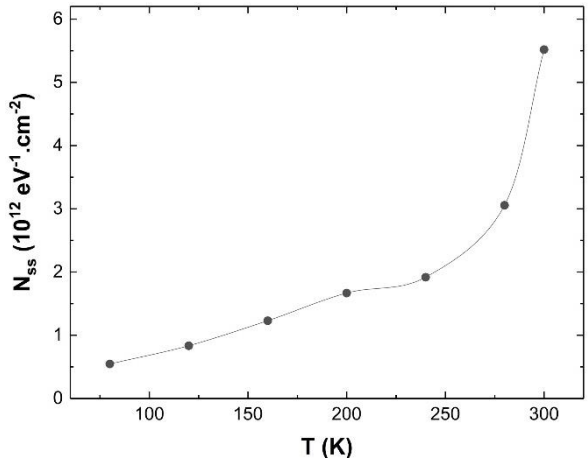

Fig. 7. N_{ss}-T graph of Au/n-GaAs contacts

4. Conclusions

Fabricated Au/n-GaAs contact's capacitance-voltage (C-V) and conductance-voltage (G/ω-V) measurements were performed in the temperature range of 80-300 K at 1 MHz frequency. The results indicate that empirical device characteristics of the metal-GaAs contacts are more complex than those considered ideal theoretical models. However, there is a good agreement between C-V-T, G/ω-V-T and R_s-V-T profiles especially in terms of the changes at/around two peak points of R_s-V profile which correspond to the intersection point in C-V profile. The observed intersection behaviour can be attributed to an inhomogeneous interfacial layer because of the interface states at the GaAs surface. However the change of interface states with temperature is probably due to increase the defects with the temperature at the semiconductor-metal interface. NC behaviour of Au/n-GaAs contact is as interesting as peak behaviour. Such behaviour of the structure could be associated with trapped charges' delocalization mechanism due to impact ionization and with the injection of charge carriers which involves a process of hopping to localized interface traps/states. Besides these, it is believed that a native interfacial layer could be formed at M/S interface and this yielded states/traps that make contribution to NC.

Acknowledgments

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